Pulse Width Modulation Harmonic Elimination Method for Common and Differential Mode Circulating Currents

Khalid Javed
Department of Electromechanical, Systems and Metal Engineering, Ghent University,
EEDT Decision & Control, Flanders Make.
Ghent, Belgium.
Khalid.Javed@UGent.be.

Lieven Vandevelde
Department of Electromechanical, Systems and Metal Engineering, Ghent University,
EEDT Decision & Control, Flanders Make.
Ghent, Belgium.
Lieven.Vandevelde@UGent.be.

Frederik De Belie
Department of Electromechanical, Systems and Metal Engineering, Ghent University,
EEDT Decision & Control, Flanders Make.
Ghent, Belgium.
Frederik.DeBelie@UGent.be.

***Abstract*— A Pulse Width Modulation method is presented in this paper for the harmonics and circulating current reduction in the power converters system. The power converter considered for this research work is a boost converter connected in an interleaved topology in a single setup. The Common-Mode Circulating Current CMCC are studied in detail in this interleaved topology setup. For the Differential-Mode Circulating Current DMCC, these two identical interleaved setups are then connected in parallel. A PWM control method is suggested for harmonic elimination and control of circulating currents inside the circuit. This method results are compared with Feed Forward and AICMC control methods. Simulation results are presented to show the effectiveness of this proposed model.**

Keywords—Circulating Currents Control, Power Electronic Converters, Harmonics Elimination.

I. INTRODUCTION

Interleaving topologies of the converters are proven to be more effective than non-interleaving because of the cancellation and reduction of first and higher-order harmonics [1]. But on the other hand, an interleaved connection between the converters generates a certain amount of unwanted currents that circulate between the interleaved converters module. Such unwanted currents in the circuit are known to be circulating currents, resulting from the difference in phase/pole voltage. To suppress the circulating currents, different types of control methods are discussed in this part of the article.

Insertion of the isolation transformer at the output end of each converter is introduced in [2] to cut the path for the flow of these unwanted currents. The problem in this method is mainly the high cost and size because of these separate isolation transformers. A Common Mode CM filter is inserted in [3] at each converter's output to suppress these circulating currents but the same problem of the high cost was the issue. In reference [4]–[8], Coupled Inductors CI is used because of its good performance in reducing circulating currents in the circuit. The only problem is these articles were the sharing of unbalanced load currents between the converters due to the insertion of these CI.

To improve the power system's capability and reliability, the converters are connected in parallel [9]–[12]. This parallel topology is also a fine way for the modularized design of the power system because it provides a flexible, high-capacity augmented system. On the other hand, paralleling the converters also have some major problems because of the unsynchronized operation of the converters connected in parallel.

Paralleling the converter device was a concept given for a more reliable system with more proper load current balancing schemes [13]–[16]. From the results of [15], [16], it is concluded that paralleling the converter is more reliable. Still, the problem of circulating current is also a major issue in such topologies [9]–[11], [13], which can also lead to the unbalanced load current sharing between the converters, which will also degrade the performance of the system. To deal with circulating currents in parallel devices can also be done via the same isolation method. The isolation can either be in the form of installing isolation transformers at the input side after the AC supply source [2], [17] or applying separated AC sources to each of the parallel-connected converters [13], [18]. The approach used in these articles is not practically desirable because of the expensiveness and bulkiness of the whole system.

In both cases, either interleaving or paralleling the converters, circulating current exist mainly because of the improper current sharing between them. While this problem of unequal current sharing mainly depends upon the control schemes applied or the mismatching of the converter parameters. So for circulating currents coping, one has to minimize these mismatches to provide a proper balanced current sharing between the converters. As isolation techniques result in bulky power systems, controlling the PWM signals approach is introduced in [19] by the researchers in which the circulating currents are eradicated from the system with the help of controlling the PWM signals provided to the converters. A similar approach is provided in [4], where the average current for each phase is calculated. Then based on these calculations, the control signals are updated for each phase individually.

Similarly, the common-mode circulating currents are controlled by Fen et al. [20], [21] considering the parallel modules as a whole, not between the phases. Another PWM control technique, i.e., the deadbeat control method [22], is introduced in which these circulating currents are controlled with the help of modifying the voltage supplied. The circulating impedance concept [21] is introduced between the converter modules to minimize the circulating currents.

A PWM control-based circulating current controller is proposed in this work for dealing with both interleaved and parallel topologies of the converter modules. In the

978-1-6654-8537-1/22/$31.00 ©2022 IEEE

beginning, all possible types of circulating current loops are identified inside the circuit in detail. The power converter selected for this article is the boost converter because of its wide and easy use in most circuits. A bridgeless interleaved topology of the two boost converters is considered in the first case. The types of the circulating current loops in this interleaved topology are discussed, along with their impact on the power system. A PWM control strategy is discussed in detail to deal with these circulating currents. This bridgeless interleaved topology of the converter module is then connected in parallel to another identical setup across a single AC power supply source. Same the possible circulating current loops are again defined in detail. Then the PWM control strategy is updated to deal with all the types of these unwanted circulating current loops. The control of circulating current loops is performed smoothly and with ease of implementation in this technique, without any communication between the parallel-connected modules. This method provides a flexible interleaved and parallel system of the boost converter with reduced size and cost. Due to the absence of the bridge in the circuit, the power losses are minimized throughout the system. According to a certain reference given voltage, the output voltage control is also maintained in this method along with harmonics reduction from the line current. The power factor of the system is also maintained near to the unity.

The distribution of the article is done as the interleaved and parallel topologies of a boost converter are discussed in section II of this paper. Our proposed control scheme is discussed in detail in section III. Section IV is about the comparison made between our controller with AICMC and Feed Forward control schemes. The detailed simulation results and comparisons are presented in section V of this article. At the end, the conclusion is made in section VI.

II. Interleaved and Parallel Connected Boost Converters

For the application of power conversion, the AC-DC conversion stage is placed immediately after an AC supply source to provide a DC voltage used furtherly for different stages. The current is drawn discontinuously from an AC source with high amplitude for a short duration. The user-end appliances demand a stable DC supply at the output. For this purpose, the capacitive filters and rectifiers are placed at the end of the circuit, resulting in short-duration current spikes. The total harmonic content of the circuit is disturbed due to this type of current spike. These types of problems are more prominent in high-power delivering circuits. For the quantitative measurement of the power quality of any power system, two main factors are monitored, i.e., Power Factor PF and Total Harmonic Distortion THD of that system. PF predominantly deals with the useful power consumption of the system. For power factor compensation, Power Factor Correctors PFCs are introduced to the power systems. PFCs tend to shape the input supply current with respect to the input supply voltage to make them in-phase and get the maximum input power from the AC supply source.

Fig. 1 illustrates a block diagram of the bridgeless PFC with the interleaved topology of a boost converter. Two boost converters are connected in an interleaved scheme for each half-line cycle. The input voltage of this circuit is symmetrical in two half-line cycles while the line current of the circuit flows only through the two diodes of the circuits, which results in low conduction losses. The space utilization and the thermal performance of the circuit also improve because of using two inductors compared to using a single conventional inductor. So it can help improve the system's efficiency even for higher power applications. The sum of both inductor currents, i.e., *IL1* and *IL2*, represents the total current from the input supply source. The ripple currents will be out of phase in these inductors, due to which they will cancel the effect of each other. This will also lead to the reduction of EMI filter size by mitigating the high-frequency ripple current generated because of the high-speed switching of the boost converter. Outer capacitor high-frequency ripple is also reduced in this interleaving technology.

The detailed operation of this bridgeless interleaved buck-boost converter is performed in two different cycles of the input voltage, i.e., the positive and the negative half cycle. During the positive half cycle, the power is transmitted from the input to the output with the use of *L1*. While for the negative half cycle, the power is supplied with the help of *L2*. For the first positive cycle, switch *S1* is ON, a path is provided for the current between the load and the input supply source with the help of inductor *L1*. The circuit loop *L1*, *S1*, and *D1* is a single boost converter switching at high frequency for the first positive cycle. For the negative half cycle, a link is provided between the input supply source and the output load with the help of inductor *L2*. Here *L2*, *S2*, and *D2* react as a boost converter switching at high frequency for another cycle.

Power electronic converter modules can be connected in parallel to increase the system's output power capabilities. Two or more power converters are connected in parallel to provide redundancy and ensure the system functionality in case of failure of a single converter. Parallel connected multiple power modules can distribute the thermal head load over a larger board area and achieve higher power requirements. As shown in the fig. 2, two identical setups of fig. 1 are considered for parallel connection. They are connected across the same supply at the input and load at the output end.

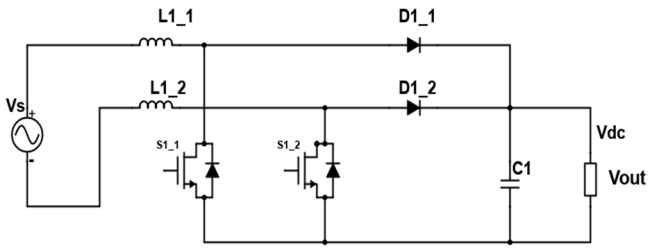

Fig. 1. Interleaved Connected Boost Converters.

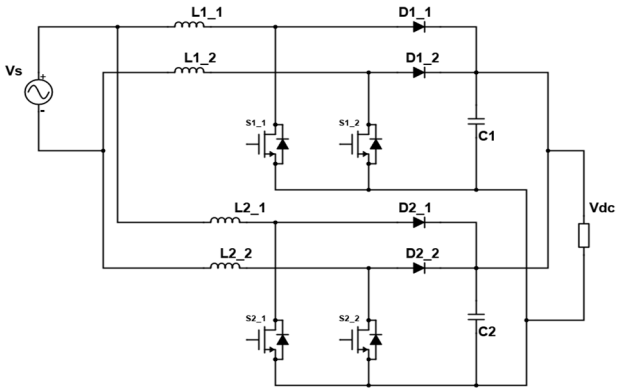

Fig. 2. Parallel Connected Two Setups of Interleaved Boost Converters.

III. Proposed Control Scheme with CMCC and DMCC Controllers

Common Mode Circulating Current CMCC refers to the types of circulating current in a single module of the interleaved topology of a boost converter. By definition, CMCC is the difference between the inductor currents of the two legs of interleaved topology [23] i.e.

$$i_{cmcc\_a} = i_{La\_1} - i_{La_2} \quad ; \quad a \in \{1, 2, 3, \dots, n\} \qquad (1)$$

A combined controller(for both interleaved and parallel connection of the converter), as shown in fig. 3 is proposed to minimize these circulating currents inside the boost converter circuit with a single module. Two main controller loops are defined inside the controller, i.e., the outer control loop and the inner control loop. The outer control loop is also known as the voltage control loop. It is specified for the output voltage regulation and to maintain it at a certain reference value. At the same time, the inner loop is also named as a current control loop, used to control the line current of the circuit. A separate CMCC controller is also added to the control part for the minimization of the common mode currents from the interleaved topology of the converter.

The Differential mode circulating currents are mainly part of the parallel-connected system, as shown in fig 2. By definition, Differential Mode Circulating Currents DMCC is the difference between the inductor currents of the first leg of each parallel-connected module i.e.

$$i_{dmcc\_jk} = \delta_j . i_{Lk\_1} - \delta_k . i_{Lm_1} \; ; \quad j, k \in \{1, 2, 3, \dots, n\}, \; j \neq m \qquad (2)$$

Here δ_x represents the distribution factor, and its value should between 0 and 1, i.e., ($0 \leq \delta x \geq 1$). This distribution factor is given by;

$$\delta_x = \frac{P_x}{P_{total}} \quad ; \quad x \in \{1, 2, 3, \dots, n\} \qquad (3)$$

P_x represents the power of that individual converter, while P_{total} represents the total power of the parallel-connected converter module system.

The below-shown controller is used in case of both parallel and interleaved connections of the converters to cope with CMCC and DMCC together. In the case of the parallel connection of the converters, the current control loop will be further divided into the number of loops depending upon the numbers of the parallel-connected setups, as shown in fig. 6. The distribution factor, shown in fig. 3 and fig. 6 will be the part of the control action performed for both CMCC and DMCC.

IV. Proposed Control Method Tradeoff with AICMC and Feed Forward Control Methods

Circulating currents in the circuits are mainly due to unbalanced current sharing between the parallel converters. Due to this unbalance in current sharing, THD of the whole power system also gets effected because of the harmonics generated in the line currents. Due to these harmonics, sometimes the supply currents become out of phase from the supply voltage, which affects the system's power factor. The proposed scheme is better in the load current sharing between the modules connected in parallel. The method presented in this article is mainly about controlling these circulating currents inside the scheme to reduce the flow of reverse currents and the harmonic generation reduction in the line currents. The above discussed control method is paralleled

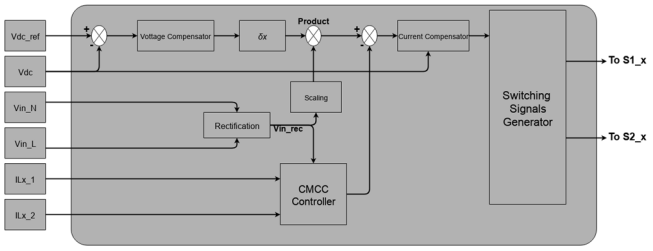

Fig. 3. Proposed Controller with both CMCC and DMCC Controller.

with two other well-known current-controlled methods, i.e., Average Inductor Current Mode Controller AICMC and Feed Forward control method.

a. Average Inductor Current Mode Controller

A well-known and easy-to-implement control scheme is AICMC. This control scheme is the most commonly used current control scheme because of its simplicity and ease of use. A general AICMC method used for this system is considered, i.e., parallel-connected modules of interleaved boost converters are shown in fig. 4. AICMC mainly comprises two control loops. The outer voltage loop works for the voltage regulation at the outer side, while the inner control loop works for the line current regulation [24].

In the outer loop, the DC output voltage is compared with a reference voltage for getting the error value, which is then provided to a PI voltage regulator to regulate the load voltage according to that specified reference voltage. After this PI regulator stage, a multiplier stage comes with two inputs, i.e., the input from the PI voltage regulator, which acts as a scaling factor for the rectified input voltage and the rectified voltage divided by the square of RMS value of input voltage. The output of this multiplier stage acts as a reference value for the current control loop where the inductor current is compared with this to produce the error signal, which is minimized by the use of the current PI regulator. All these stages require a high-speed DSP where the processes are performed continuously with the help of software in each cycle.

b. Feed Forward Control Scheme

The Feed Forward control algorithm for the scheme, taken under consideration in this research work, is shown in fig. 5. The feed forward control is about the calculation of the duty cycle values responsible for the system's unity power factor [25], [26]. For input voltage $V_{in}(t)$, output voltage $V_{out}(t)$, $d(n)$ as duty cycle for n^{th} switching cycle, $t(n)$ and $t(n+1)$ as the beginning instant of n^{th} and $(n+1)^{th}$ switching cycle and T_s as the switching period, the equations for the ON and OFF state of conventional boost converters are given by equation (4) and (5) respectively;

$$V_{in}(t(n)) = L \frac{i_L(t(n) + d(n).T_s) - i_L(t(n))}{d(n).T_s} \qquad (4)$$

$$V_{in}(t(n)) - V_o(t(n)) = L \frac{i_L(t(n+1)) - i_L(t(n) + d(n).T_s) - i_L(t(n))}{d(n).T_s} \qquad (5)$$

From above two equations, the inductor currents at the beginning of the next switching cycle can be deduced from inductor current at the beginning of present switching cycle;

$$i_L(t(n+1)) = i_L(t(n)) + \frac{V_{in}(t).T_s}{L} - \frac{V_o(n)(1 - d(n)).T_s}{L} \qquad (6)$$

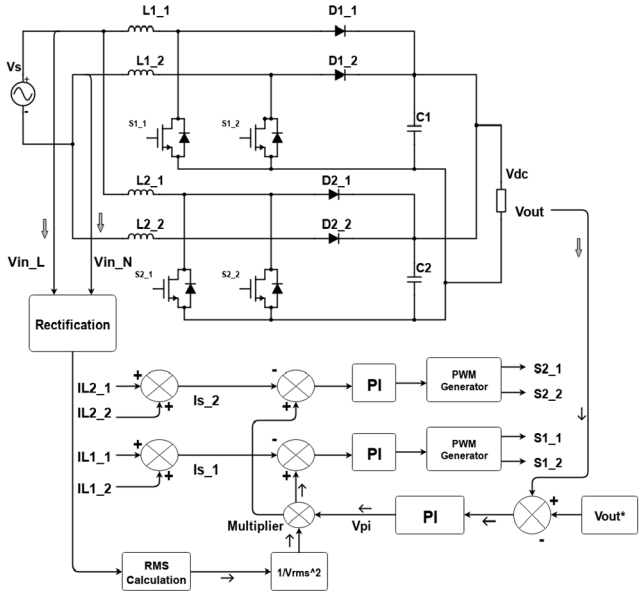

Fig. 4. AICMC Control Scheme for under-considered Parallel Power System.

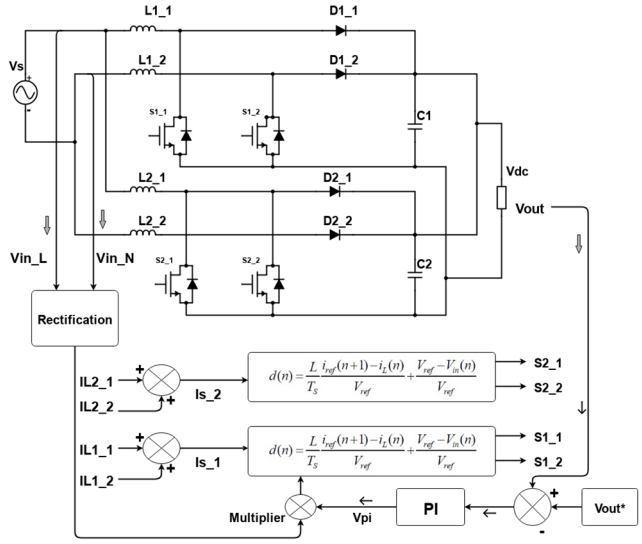

Fig. 5. Feed Forward Control Scheme for under-considered Parallel Power System.

So based on the circuit parameters of the conventional boost converter, the duty cycle value for the unity power factor can be deducted from the equation (6);

$$d(n) = \frac{L(i_L(n+1) - i_L(n))}{V_o . T_s} + \frac{V_o - V_{in}(n)}{V_o} \qquad (7)$$

The results of these two schemes are presented in the next section of simulation results. Then their comparison is made with our proposed control method, which is the main theme of this research work. The effectiveness and the better performance of our proposed PWM-based harmonics elimination and circulating current reduction is presented in the next section of this article.

V. Simulations and Results Comparison

This setup contains four boost converters, each in a set of two connected in bridgeless interleaved topology to provide a single module. Then these two modules are connected in parallel topology. The verification of our proposed scheme is done with the help of MATLAB. Interleaved Topology

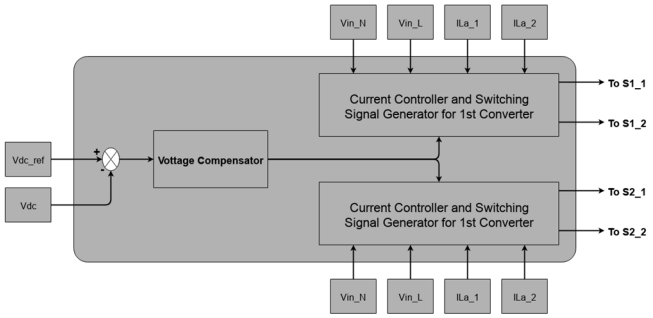

Fig. 6. Centralized Controller.

circuit of two converters is used to verify Common Mode Circulating Currents CMCC control. Two such interleaved topology modules are connected in parallel to perform the verification of the Differential Mode Circulating Currents DMCC control. A centralized scheme shown in fig. 6 is verified in Simulink for two modules of the bridgeless boost interleaved converters connected in parallel to each other, which can be extended to the *n* numbers of parallel-connected converter modules. For verifications and comparison, this proposed scheme is compared with the simulation of the same scheme with other well-known control methods, i.e., Average Inductor Current Mode Controller AICMC and Feed Forward control method.

Before applying the control to interleaved and parallel converters, their profile for the CMCC is shown in fig. 7. It shows the CMCC profile and both inductor currents of the same modules, with no control applied. Similarly, the DMCC currents profile, which is the difference between the first leg of each parallel module without any controller is shown in fig. 11. It can be seen that without control, there are harmonics as well as circulating currents in these interleaved and parallel-connected converters.

Now for comparison, all three control schemes shown in fig. 3, fig. 4, and fig. 5 are applied to the system to verify our proposed method adequately. The result comparisons are performed to show the efficiency and tenacity of our proposed work in terms of the harmonics elimination, power factor improvement, and all the types of circulating currents reduction from the system that are dangerous for these converters. The sequence followed is; Applying AICMC first, followed by the Feed Forward controller and then our proposed control scheme at the end. The results are provided first for CMCC and then for DMCC for the above three controllers.

Following the sequence, the AICMC, Feed Forward and our proposed controller results for CMCC are shown in fig. 8, fig. 9, and fig. 10, respectively. In the case of AICMC and Feed Forward controller, there still exist common-mode circulating currents inside the system. In the case of our proposed scheme, these circulating currents are efficiently removed from the system, as shown in fig. 10. Similarly, following the sequence for DMCC, the results shown in fig. 12-14 shows the differential mode circulating currents profile for AICMC, Feed Forward, and our proposed control method. It is prominent that our proposed control scheme has a proper control on DMCC. The inductor currents profile for DMCC controller and input supply voltage and current profiles are shown in fig. 15 and 16 respectively. It is evident that both the voltage and current are purely sinusoidal, and they are in phase to each other resulting in low THD of the system.

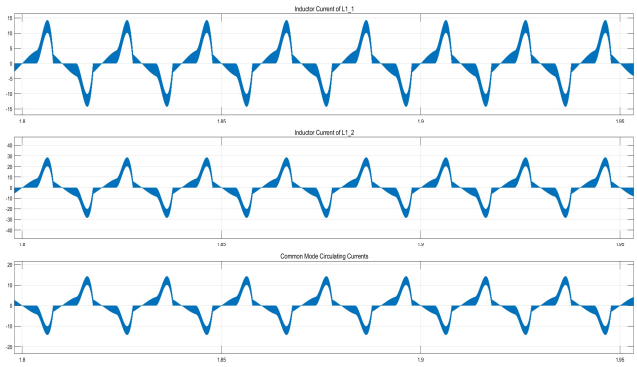

Fig. 7. CMCC Profile w/o any Controller along with Inductor Currents.

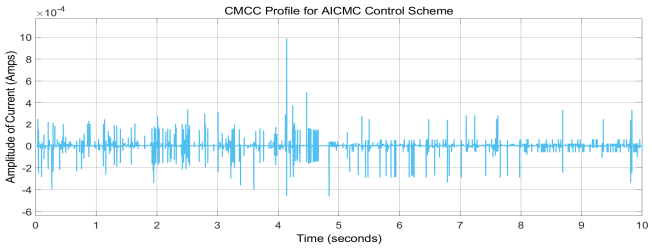

Fig. 8. CMCC Profile with AICMC Control Method.

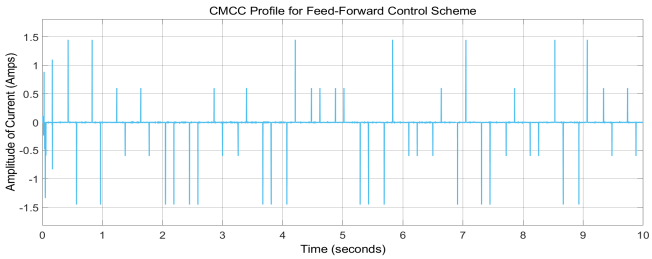

Fig. 9. CMCC Profile with Feed Forward Control Method.

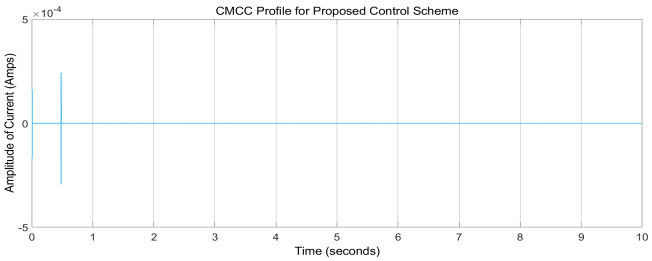

Fig. 10. CMCC Profile with proposed controller method.

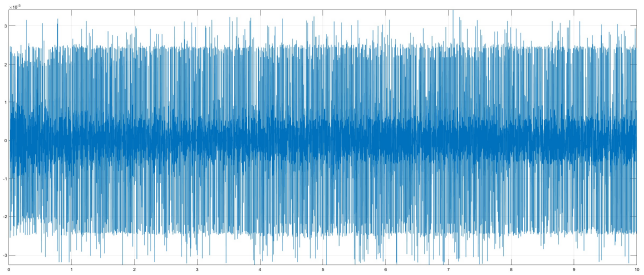

Fig. 11. DMCC Profile w/o any Control.

Summing up all the results and discussions, it has been proved that our proposed scheme is performing better in terms of the other two methods. If we dig further into the results, we can say that after our proposed control scheme, the second-best performance for this power system setup is shown by AICMC, which controls both CMCCs and DMCCs to a certain extent to Feed Forward control scheme.

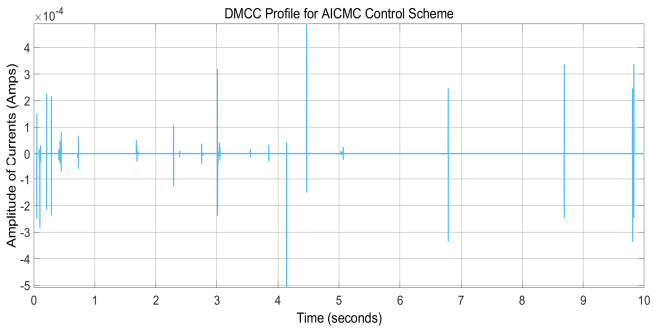

Fig. 12. DMCC Profile with AICMC Control Method.

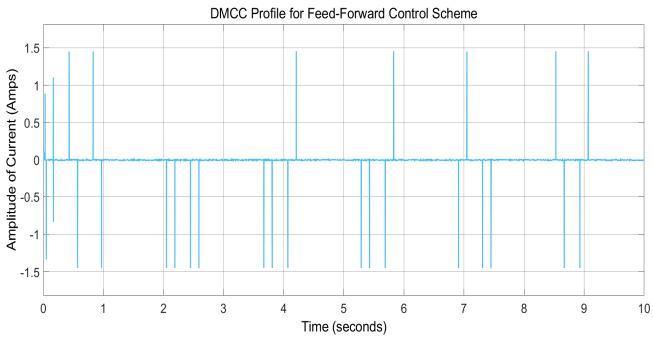

Fig. 13. DMCC Profile with Feed Forward Control Method.

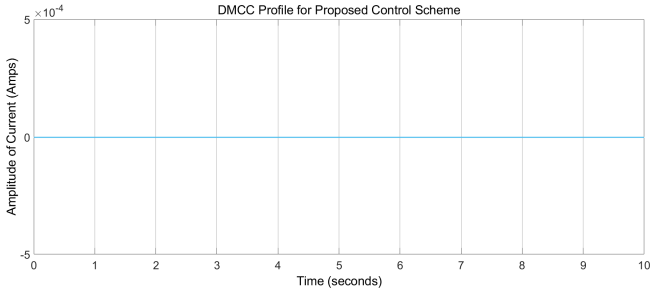

Fig. 14. DMCC Profile with DMCC Controller.

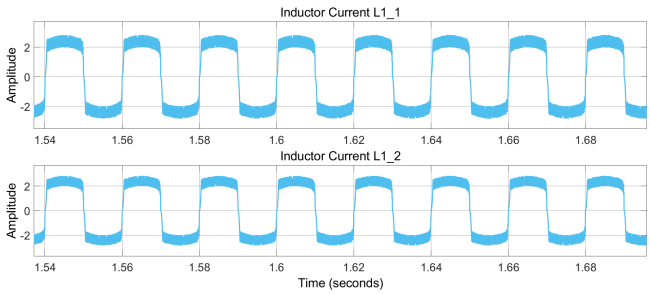

Fig. 15. Inductor Current profile for Proposed Control Scheme.

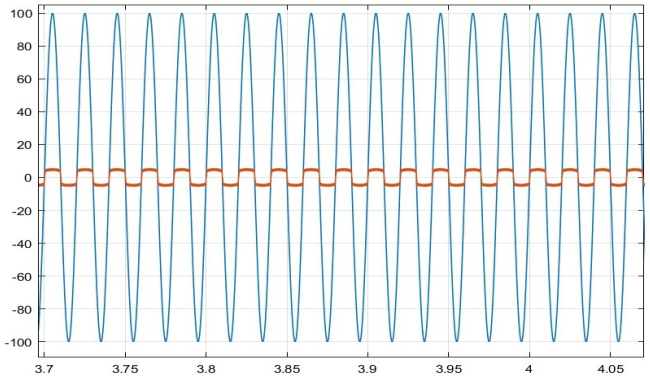

Fig. 16. Supply Voltage and Current Profile.

VI. Conclusion

A control method is proposed in this research work to reduce the circulating current in different topologies of the power converters. The circulating currents existing in interleaved and parallel connections of the converters are discussed in detail. Then two other controllers and our proposed controller are applied to it to minimize both common mode and differential mode circulating currents. The result comparisons clearly show the effectiveness of our proposed controller.

References

[1] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, 'Line Filter Design of Parallel Interleaved VSCs for High-Power Wind Energy Conversion Systems', IEEE Transactions on Power Electronics, vol. 30, no. 12, pp. 6775–6790, Dec. 2015, doi: 10.1109/TPEL.2015.2394460.

[2] J. W. Dixon and B. T. Ooi, 'Series and parallel operation of hysteresis current-controlled PWM rectifiers', IEEE Transactions on Industry Applications, vol. 25, no. 4, pp. 644–651, Jul. 1989, doi: 10.1109/28.31241.

[3] L. Asiminoaei, E. Aeloiza, P. N. Enjeti, and F. Blaabjerg, 'Shunt Active-Power-Filter Topology Based on Parallel Interleaved Inverters', IEEE Transactions on Industrial Electronics, vol. 55, no. 3, pp. 1175–1189, Mar. 2008, doi: 10.1109/TIE.2007.907671.

[4] G. J. Capella, J. Pou, S. Ceballos, J. Zaragoza, and V. G. Agelidis, 'Current-Balancing Technique for Interleaved Voltage Source Inverters With Magnetically Coupled Legs Connected in Parallel', IEEE Transactions on Industrial Electronics, vol. 62, no. 3, pp. 1335–1344, Mar. 2015, doi: 10.1109/TIE.2014.2345345.

[5] D. Shin et al., '1.5MVA grid-connected interleaved inverters using coupled inductors for wind power generation system', in 2013 IEEE Energy Conversion Congress and Exposition, Sep. 2013, pp. 4689–4696. doi: 10.1109/ECCE.2013.6647330.

[6] G. Gohil, L. Bede, R. Maheshwari, R. Teodorescu, T. Kerekes, and F. Blaabjerg, 'Parallel interleaved VSCs: Influence of the PWM scheme on the design of the coupled inductor', in IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society, Oct. 2014, pp. 1693–1699. doi: 10.1109/IECON.2014.7048730.

[7] D. Shin, K.-J. Lee, H.-J. Kim, J.-P. Lee, T.-J. Kim, and D.-W. Yoo, 'Coupled inductors for parallel operation of interleaved three-phase voltage source grid-connected inverters', in 2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Mar. 2013, pp. 2235–2239. doi: 10.1109/APEC.2013.6520606.

[8] D. Shin, J.-P. Lee, D.-W. Yoo, and H.-J. Kim, 'Stability Improvement of Interleaved Voltage Source Inverters Employing Coupled Inductors for Grid-Connected Applications', IEEE Transactions on Industrial Electronics, vol. 62, no. 10, pp. 6014–6023, Oct. 2015, doi: 10.1109/TIE.2015.2420044.

[9] C.-T. Pan and Y.-H. Liao, 'Modeling and Coordinate Control of Circulating Currents in Parallel Three-Phase Boost Rectifiers', IEEE Transactions on Industrial Electronics, vol. 54, no. 2, pp. 825–838, Apr. 2007, doi: 10.1109/TIE.2007.891776.

[10] Z. Ye, D. Boroyevich, J.-Y. Choi, and F. C. Lee, 'Control of circulating current in two parallel three-phase boost rectifiers', IEEE Transactions on Power Electronics, vol. 17, no. 5, pp. 609–615, Sep. 2002, doi: 10.1109/TPEL.2002.802170.

[11] C. B. Jacobina, E. C. dos Santos, N. Rocha, B. de Sá Gouveia, and E. R. C. da Silva, 'Reversible AC Drive Systems Based on Parallel AC–AC DC-Link Converters', IEEE Transactions on Industry Applications, vol. 46, no. 4, pp. 1456–1467, Jul. 2010, doi: 10.1109/TIA.2010.2049724.

[12] C.-T. Pan and Y.-H. Liao, 'Modeling and Control of Circulating Currents for Parallel Three-Phase Boost Rectifiers With Different Load Sharing', IEEE Transactions on Industrial Electronics, vol. 55, no. 7, pp. 2776–2785, Jul. 2008, doi: 10.1109/TIE.2008.925647.

[13] T. Kawabata and S. Higashino, 'Parallel operation of voltage source inverters', IEEE Transactions on Industry Applications, vol. 24, no. 2, pp. 281–287, Mar. 1988, doi: 10.1109/28.2868.

[14] J. Holtz, W. Lotzkat, and K.-H. Werner, 'A high-power multitransistor-inverter uninterruptable power supply system', IEEE Transactions on Power Electronics, vol. 3, no. 3, pp. 278–285, Jul. 1988, doi: 10.1109/63.17945.

[15] N. Seki and H. Uchino, 'Which is better at a high power reactive power compensation system, high PWM frequency or multiple connection?', in Proceedings of 1994 IEEE Industry Applications Society Annual Meeting, Oct. 1994, vol. 2, pp. 946–953 vol.2. doi: 10.1109/IAS.1994.377532.

[16] L. Matakas, C. Burlacu, and E. Masada, 'The connection of converters instead of semiconductor power devices — a high performance solution for the mva range of power comverters', J CIRCUIT SYST COMP, vol. 05, no. 03, pp. 503–521, Sep. 1995, doi: 10.1142/S021812669500031X.

[17] Y. Komatsuzaki, 'Cross current control for parallel operating three phase inverter', in Proceedings of 1994 Power Electronics Specialist Conference - PESC'94, Jun. 1994, vol. 2, pp. 943–950 vol.2. doi: 10.1109/PESC.1994.373793.

[18] C. S. Lee et al., 'Parallel UPS with a instantaneous current sharing control', in IECON '98. Proceedings of the 24th Annual Conference of the IEEE Industrial Electronics Society (Cat. No.98CH36200), Aug. 1998, vol. 1, pp. 568–573 vol.1. doi: 10.1109/IECON.1998.724306.

[19] S. Ji, Y. Yong, and Q. Chunqing, 'Control of circulating current for direct parallel grid-connected inverters in photovoltaic power generation', in 2009 International Conference on Mechatronics and Automation, Aug. 2009, pp. 3805–3810. doi: 10.1109/ICMA.2009.5246756.

[20] F. Tang, X. Jin, Y. Tong, J. Liu, F. Zhou, and L. Ma, 'Parallel interleaved grid-connected converters in MW-level wind power generation', in 2009 IEEE International Electric Machines and Drives Conference, May 2009, pp. 789–796. doi: 10.1109/IEMDC.2009.5075294.

[21] M. Yu et al., 'A Novel Decoupled Current-Sharing Scheme Based on Circulating-Impedance in Parallel multi-Inverter System', in IECON 2007 - 33rd Annual Conference of the IEEE Industrial Electronics Society, Nov. 2007, pp. 1668–1672. doi: 10.1109/IECON.2007.4460122.

[22] H. Xiao, A. Luo, L. Bai, C. Tu, J. Zhou, and Q. Liu, 'A deadbeat control method for circulating current between parallel-connected inverters', in 2013 1st International Future Energy Electronics Conference (IFEEC), Nov. 2013, pp. 806–811. doi: 10.1109/IFEEC.2013.6687612.

[23] Y.-H. Liao, H.-C. Chen, H.-C. Cheng, Y.-L. Ke, and Y.-T. Li, 'A Novel Control Strategy of Circulating Currents in Paralleled Single-Phase Boost Converters With Different Power Sharing for Microgrid Applications', IEEE Transactions on Industry Applications, vol. 50, no. 2, pp. 1304–1312, Mar. 2014, doi: 10.1109/TIA.2013.2289995.

[24] D. Jayahar and R. Ranihemamalini, "Inductor Average Current Mode Control for single phase Power Factor Correction Buck-Boost Converter," 2011 International Conference on Emerging Trends in Electrical and Computer Technology, 2011, pp. 274-279, doi:10.1109/ICETECT.2011.5760128.

[25] Azazi, H.Z., El-Kholy, E.E., Mahmoud, S.A. and Shokralla, S.S., 2010, December. Digital control of boost PFC AC-DC converters with predictive control. In 14th International Middle East Power system Conference (MEPCON'10), Egypt (pp. 721-727).

[26] K. Javed, L. Vandevelde and F. De Belie, "Duty Ratio Calculation for Digitally Feed Forward Controlled Parallel Connected Buck-Boost PFC," 2020 IEEE International Conference on Environment and Electrical Engineering and 2020 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I&CPS Europe), 2020, pp. 1-6, doi: 10.1109/EEEIC/ICPSEurope49358.2020.9160656.