LETTER

A Low-Power Reduced Kick-Back Comparator with Improved Calibration for High-Speed Flash ADCs

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SUMMARY A novel low-power kick-back reduced comparator for use in high-speed flash analog-to-digital converters (ADC) is presented. The proposed comparator combines cascode transistors to reduce the kick-back noise with a built-in threshold voltage to remove the static power consumption of a reference. Without degrading other figures, the kick-back noise is reduced by a factor 8, compared to a previous design without cascode transistors. An improved calibration structure is also proposed to improve linearity when used in an ADC. Simulated in a standard CMOS technology the comparator consumes 106.5 μ W at 1.8 V power supply and 1 GHz clock frequency.

key words: comparator, kick-back, calibration, low-power, flash ADC

1. Introduction

Today's high data rates necessitate the use of high-speed flash Analog-to-Digital Converters (ADC). The performance of these converters in terms of speed, power-consumption, and linearity greatly depends on the architecture of the comparators used. Standard ADC designs consist of an input-buffer/track and hold amplifier, a reference ladder and a sense amplifier or S/R-type track and latch comparator. In [1], a low power high-speed ADC design was proposed, based on a switched type sense amplifier with built-in reference voltages. This omits the use of a reference ladder and reduces the static power dissipation, yielding 10.6 mW of power consumption at 1 Gs/s and 4-bit resolution. A down-side of this design is that comparator switching generates considerable kick-back noise into the ADC input, which necessitates the use of a low-impedance buffer for driving the ADC, and so the overall power reduction of this system is limited. Other comparators [2], [3] have been proposed with low kick-back noise. However, these approaches show a relatively high power consumption due to the need for a static reference ladder or due to a folded architecture. This paper presents a comparator using the best of the two worlds: cascode transistors to reduce the kick-back noise while maintaining the low power consumption and removing the need of a static reference ladder due to offsetting the input transistors.

2. Differential Comparator

Paper [1] presents a novel comparator architecture for a low power, high speed ADC. By using transistors with offset widths ($W_0 \pm \Delta W$) in the input differential pair, the need for a reference voltages is omitted, reducing the power consumption. The resulting offset voltage can be expressed as a first-order approximation, Eq. (1).

$$\Delta V_{th} = \frac{V_{GS} - V_{Tn}}{2} \frac{\Delta W}{W} \quad (1)$$

Due to process and mismatch variations a large variation in threshold voltage (V_{Tn}) can be expected, compared to the LSB of the ADC, and this needs to be calibrated. An array of binary-scaled switchable capacitors (C) connected to the drains of the input NMOS transistors can be used. The variation in voltage can be expressed as

$$V_{OD} = \frac{V_{GS} - V_{Tn}}{2} \frac{\Delta C}{C}. \quad (2)$$

As stated in the introduction, a downside of the comparators used in this circuit is the significant amount of kickback noise injected into the input nodes when the clock switches. This noise is caused by large voltage and current variations at the input NMOS transistor pair when the comparator is switched on or off. These variations result in charge pulling or pushing to the input-nodes via the gate-drain and gate-source capacitances of the input pair.

These charges are converted into voltages over the output impedance of the driving stage. This results in a change of the input voltage at the very moment the comparator is switched on, the moment when it is most sensitive. Or even worse: the voltage change caused by the switching off of the comparator may not have disappeared before the next cycle, resulting in a memory effect making the state of the comparator depend on its previous state rather than solely on the actual input voltage. These effects reduce the accuracy of the ADC and increase the need for a low-impedance drive stage, consuming a considerable amount of power as the low impedance must be maintained up to and above the ADC clock frequency.

3. Proposed Comparator

To reduce the overall power consumption, including the

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Fig. 1 The proposed comparator.

driver, one needs to reduce the kick-back noise. A straightforward way to realize this is adding a source follower to the input transistors [3]. However, this not only adds static power consumption, but also increases the thermal noise. The proposed comparator shown in Fig. 1 is a better approach. It is less effective in terms of kick-back noise reduction compared to [3], but the reduction is significant, and it does not increase the input noise nor the power consumption. This architecture reuses the idea of offsetting the widths of the input NMOS transistors of the comparators to induce an offset voltage and eliminate the reference ladder, and combines it with cascode transistors [2] to isolate the input differential pair from the regenerative part, and reduce the fast voltage swings across the input transistors. These cascodes separate the calibration capacitors from the drain-gate capacitors of the input differential pair, eliminating the large charge injections to the input nodes and improving the comparator sensitivity, effectively reducing the kick-back noise to clock feed through.

4. PMOS Capacitor

Thanks to the improved sensitivity a more accurate calibration can be applied. In [1] the switchable capacitors are implemented as PMOS capacitors, so that the minimum calibration step is determined by the minimum size of a transistor. To reduce the minimum calibration step the circuit in Fig. 2 is proposed. The operation of the device can be explained when looking at the different phases in the comparison. In the first phase—as the clock makes a transition from low to high—the lower transistors start sinking current out of the calibration capacitors which were charged to the supply voltage. As the transistors can be replaced with their g_m , the voltage on X can be expressed as $v_X(t) = V_{DD} \exp(-t g_m/C)$. As soon as the voltage on one of the branches drops below the threshold voltage of the NMOS transistors of the regenerative part, the positive feedback starts to work and the comparator goes to a fixed state. The capacitance of the calibration capacitors—implemented as PMOS transistors with drain and source connected to node X—can be changed by changing the gate

Fig. 2 Variable PMOS capacitor.

voltage. If the gate-source voltage is higher than the threshold voltage (V_{Tp}), the capacitance is approximately equal to the oxide capacitance (C_{ox}). If the gate-source voltage is lower than V_{Tp} , the channel in the PMOS is formed and its capacitance (C_{ch}) comes in series with C_{ox} , resulting in a total capacitance of $C_L = \frac{1}{1/C_{ox} + 1/C_{ch}}$. This mechanism is used to change the total capacitance on node X in [1]. The smallest step size of the capacitance is achieved when switching the channel of a minimum size PMOS capacitor on and off. Thus, the gate voltage (V_G) of such a minimum size capacitor can be set between the 2 logical values. When V_G is lower than $V_{DD} + V_{Tp} - V_{Tn}$ the channel is never pinched off; when V_G is larger than $V_{DD} + V_{Tp}$ the channel can never be formed. In between these states the capacitance at the starting of phase 1 of the comparison is equal to C_L but as soon as the voltage on node X drops below $V_G + V_{Tp}$ the capacitance is changed to C_{ox} . This results in an average capacitance between C_{ox} and C_L which has been simulated and modeled as in Eq. (3).

$$C(V) = \begin{cases} C_{ox} : V_G > V_{DD} + V_{Tp} \\ -\frac{C_{ox}/V_{Tn}}{C_{ch}/C_{ox} + 1}(V_{DD} + V_{Tp} - V_G) + C_{ox} : \\ V_{DD} + V_{Tp} - V_{Tn} < V_G < V_{DD} + V_{Tp} \\ (\frac{1}{C_{ox}} + \frac{1}{C_{ch}})^{-1} : V_G < V_{DD} + V_{Tp} - V_{Tn} \end{cases} \quad (3)$$

By choosing the gate voltage such that a linear change in capacitance results, a more accurate calibration can be obtained. This results in a more accurate DNL and INL increasing the performance of the ADC. In Fig. 2 4 different voltages can be applied, but as can be seen, this technique can be generalized to more bits.

5. Simulation Results

The proposed comparator was simulated in a 0.18- μm CMOS technology at 1.8 V supply and driven by a 1 GHz clock. To measure the kick-back noise, the input gate voltage is measured over a 1 k Ω resistor inserted between the input transistors (V_{in-} , V_{in+}) and the differential voltage source. In Fig. 3 the differential and common-mode kick-back noise is displayed for the proposed comparator and for the reference design of [1]. The voltages are measured for a differential input signal of 100 mV. This figure shows

Table 1 Comparison of the key figures.

	Proposed Comparator	[1]	[2]	[3]
Technology (CMOS)	0.18 μm	0.18 μm	90 nm	0.18 μm
Common kick-back charge (aC/cycle)	235.91	309.53	182	-
Differential kick-back charge (aC/cycle)	11.99	92.51	-	-
Power Dissipation (μW)	106.5	138.7	27.9	202
Sampling frequency (GHz)	1	1	1	0.25
Input-referred Thermal Noise (1σ in mV)	0.66	0.5	-	-

Fig. 3 (a) The common-mode and (b) differential voltage swing due to kick-back over a 1 k Ω resistor connected at the input gates. **Fig. 4** The voltage swings at (a) the source node of the input transistors and at (b) the drain node of the input and cascode transistor.

that the differential kickback at the sampling events (0, 1 and 2 ns) is significantly reduced. The simulations show that the voltage swings at the drain and source of the input NMOS transistors are reduced (Fig. 4). The main voltage swings now occur over the cascode transistors isolating kick-back charges from the inputs. Figure 4 also shows that the common-mode kick-back voltage is inverted compared to the reference design as the drain capacitor of the input transistors is charged to ground instead of V_{DD} .

In Table 1 the resulting figures are compared. The differential kickback is 8 times smaller, whereas the power consumption is reduced by 25%, compared to [1]. The kickback reduction relaxes the requirements on the output impedance of the preceding amplifier stage, resulting in an additional reduction of the overall power consumption. The

input noise is still comparable with the reference design. For a 1 GHz clock and 200 mVpp input range, this input noise results in 3.8 effective bits (ENOB) for a 4-bit ADC design, or 5.2 ENOB for a 6-bit ADC design. The performance of [2] is comparable, keeping the technology scaling in mind, however the stated power consumption does not yet include the power consumption of the reference ladder. The kickback of [3], though not mentioned, is lower than in the proposed design. However, this technique consumes two times more power at a much lower sampling frequency (250 MHz).

6. Conclusion

An improved comparator for use in high-speed, low-power Analog-to-Digital Converters was presented. A significant reduction of kick-back noise was obtained, without a penalty in the performance or the power consumption. The reduction in kick-back noise was achieved by placing switched cascode transistors between the differential input stage and the regenerative stage of the comparator. This reduction of kick-back noise relaxes the requirements of the ADC driver stage which results in an overall decrease of the power consumption. A more accurate calibration structure is also proposed to improve the linearity in higher resolution ADC designs, making the comparator useful for 6-bit resolution 1 Gsps ADCs in the given technology.

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