PAPER

Design of Automotive VCSEL Transmitter with On-Chip Feedforward Optical Power Control

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SUMMARY We propose a novel 50 Mb/s optical transmitter fabricated in a 0.6 μm BiCMOS technology for automotive applications. The proposed VCSEL driver chip was designed to operate with a single supply voltage ranging from 3.0 V to 5.25 V. A fully integrated feedforward current control circuit is presented to stabilize the optical output power without any external components. The experimental results show that the optical output power can be stable within a 1.1 dB range and the extinction ratio greater than 14 dB over the automotive environmental temperature range of -40°C to 105°C .

key words: driver circuits, integrated circuits, feedforward systems, surface-emitting lasers

1. Introduction

Data networks in the car are taking the form of a fiber optical network, due to its important advantages such as lower weight, higher data rates and low emission of electromagnetic interference [1].

In this paper, we present a novel VCSEL driver that was designed to handle the hostile automotive environment. The main difficulties to overcome are the requirements of a wide environmental temperature range (from -40° to 105°C), and a very wide supply voltage range (from 3.0 V to 5.25 V, providing flexibility in power supply selection in cars) combined with very low-cost requirements (e.g. no external components and 5-pin package restriction). The optical transmitter consists of a driver circuit and a 850 nm VCSEL. It has to emit a stable optical output power with a narrow tolerance to meet the optical power budget requirement of the link and to reduce the receiver dynamic range. Traditional drivers employ a photodiode that is coupled to the laser's backfacet for monitoring the optical output power, forming an automatic power control loop [2]. Although the feedback approach inherently has better long-term performance, most VCSELs do not possess a backfacet photodiode, making the use of a feedback loop difficult. In [3], a transceiver is presented based on the flip-chip bonding of VCSEL and PIN arrays onto silicon-on-sapphire. This allows a silicon detector to monitor each VCSEL. However, the silicon-on-sapphire technology is still costly, which lim-

its its use in automotive applications. A feedforward scheme including an off-chip variable resistor is proposed in [4], but it requires an additional IO pin and is not cost-effective. Here, pure on-chip feedforward compensation of the temperature dependence and calibration of the process dependence were used to stabilize the optical output power of the VCSEL.

2. Transmitter Architecture

Figure 1 shows the required dc-current needed to maintain constant optical output power with temperature [5]. As can be seen, this curve can be approximated by a piecewise linear function. When transmitting data, the VCSEL current consists of the bias current (the applied current during transmission of a '0') and the modulation current (the difference in applied current between transmission of a '1' and a '0'). In our feedforward compensation scheme, shown in Fig. 2, this bias current is kept constant with temperature, and characterized by the parameter I_b . The generated modulation current is piecewise linear, and can be characterized by the initial value I_0 , the threshold temperature T_0 and the temperature coefficient TC of the linear part of the modulation current. These four parameters must be chosen differently for each VCSEL, and also depend upon the process corner of each chip. Therefore, these parameters are digitally adjustable via zap cells, which are set during a calibration procedure. During the calibration procedure the parameters must be set such that the eye-safety limit (less

Fig. 1 Typical VCSEL currents versus junction temperature.

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Fig. 5 Schematic of the VCSEL driver stage.

3.2 VCSEL Output Driver

To reduce costs, no external ac-coupling capacitance can be used in this design. Therefore, the VCSEL is dc-coupled to the driver (Fig. 5). Of major concern for any dc-coupled laser or VCSEL driver is the headroom left to drive the VCSEL at the lowest supply voltage (i.e. 3.0 V) to drive the VCSEL. Here, this problem was solved by employing the common cathode configuration [7], using the threshold voltage of the VCSEL itself to bias the collector voltage of the differential pair.

A key problem in this design is the fact that the input common-mode voltage of the input buffer is referred to the supply voltage, which ranges from 3.0 V to 5.25 V. Hence, given the associated wide common-mode swing, this signal cannot be directly applied to the differential output pair because signals with common-mode voltage larger than $V_{VCSEL} + V_{sat,Q2}$ will saturate the bipolar transistor Q_2 in the driver stage. Therefore, we used a pMOS differential pair (M_1, M_2) to refer the common-mode voltage to ground. The common-mode voltage at the input of the driver stage is given as,

$$V_{CM,driver} = I_{SS}(R_0 + R_1/2) + V_{GS3}. \quad (3)$$

It is independent from the supply voltage (which can vary by more than 2 V), and is determined by the tail current I_{SS} , load resistors of the pMOS differential pair (M_1, M_2) and level shifter M_3, M_4 .

3.3 Bias Current Generator

Using an on-chip bandgap reference, one can easily produce a voltage that shows little dependence upon temperature, process corners and the supply voltage. Typically, one then generates a precision current using this band-gap voltage and an external precision resistor. However, this requires an additional I/O pin and an external resistor, which is not available. As the absolute value of an on-chip resistor varies a lot with process corners (about $\pm 30\%$), any current derived from a bandgap voltage and an on-chip resistor has the same process dependency as this resistor.

As these process variations result in unacceptable tolerances on the emitted optical output power, they are removed via a calibration procedure. As shown in Fig. 6 a

Fig. 6 Schematic of bias current generation.

so-called process calibration cell first removes the process dependency by generating the current I_{cal} :

$$\begin{aligned} I_{cal} &= I_0 + Cal[1] \cdot I_1 + \dots + Cal[8] \cdot I_8 \\ &= (k_0 + Cal[1] \cdot k_1 + \dots + Cal[8] \cdot k_8) \cdot I_{CONST} \\ &= K_{cal} \cdot I_{CONST} \end{aligned} \quad (4)$$

where $Cal[1 : 8]$ is an 8-bit calibration value, which can be set by the zapping circuits, and $k_0, \dots, k_8$ are the current mirror ratio of each branch (in our case unit ratios are used for simplicity). I_{CONST} is a constant-to-temperature current derived from an on-chip bandgap and an on-chip resistor. By setting the calibration value (thus the ratio K_{cal}), one can calibrate the output reference current to a process-independent value. The high-swing cascode current mirrors are used here for higher output resistance and low-voltage operation [8]. After the process calibration, another stage of calibration cells with different current ratios (K_{Ib}) is used for setting the Ib parameter for the bias current. The final output bias current is $I_{BIAS} = K_{Ib} I_{cal} = K_{Ib} K_{cal} I_{CONST}$, where K_{cal} and K_{Ib} can each be set with a value from 1 to 8.

3.4 Modulation Current Generator

The piecewise linear modulation current is determined by three parameters: the initial value I_0 , the threshold temperature T_0 and the temperature coefficient TC of the linear part of the modulation current. Figure 7 shows the diagram of modulation current generator. The circuit is composed of two current generators (upper branch and lower branch), generating respectively I_{upper} and I_{lower} .

The upper branch generates a current with the desired T_0 and TC settings, which are temperature dependent. The temperature information is derived from a proportional-to-absolute-temperature (PTAT) current source. The first step is to introduce the T_0 cross-point into I_{upper} . This is done by subtracting a calibrated constant-to-temperature current (I_{CONST}) from a PTAT current (I_{PTAT}) via current mirrors.

Fig. 7 Diagram of modulation current generation.

Fig. 8 Diagram of zapping circuit.

The resulting current I_{To} is given as,

$$I_{To} = \begin{cases} K_3(K_2 I_{PTAT} - K_1 K_{To} I_{CONST}), & \text{if } T \leq T_o \\ 0, & \text{otherwise} \end{cases} \quad (5)$$

where K_1 , K_2 and K_3 are the current mirror ratios, and T_o is the temperature point that makes $K_2 \cdot I_{PTAT} = K_1 \cdot K_{To} \cdot I_{CONST}$. Because the I_{PTAT} and I_{CONST} have the same process dependency and K_1 , K_2 are fixed, the resulting zero cross-point T_o is only dependent on K_{To} in the first order. I_{To} is then calibrated with the process calibration cell and TC calibration cell is used to set the temperature coefficient of the modulation current.

The lower branch, which sets I_o , has a similar structure as the bias current generator. Finally the upper and lower currents are added together to form the piecewise linear modulation current.

3.5 Zapping Circuit

The zapping circuit is used to set the digital calibration settings (Cal , Ib , I_o , T_o , and TC) used in the bias and modulation current generators. As shown in Fig. 8, it consists of control logic and Zener cells. In each Zener cell, a Zener diode is controlled by a “selection transistor,” e.g., nMOS transistors M_1 , M_2 , ... in Fig. 8. The “selection signals” applied at the gate of the selection transistors are correspond-

Fig. 9 Flow chart of two-step calibration procedure.

ing to the digital calibration settings for the transmitter.

Before a transmitter is put into operation, there is a two-step calibration procedure to compensate for the silicon and VCSEL process corners. As shown in Fig. 9, in the first step (the configuration step), we first calculate the required calibration settings based on the algorithm described in Sect. 4, and then the “Program” and “Data input” pins are used to send user-defined configuration commands to the control logic. The control logic then drives the gates of the selection transistors using the selection signals (i.e., the calibration setting values).

In the second step (the zapping step), the voltage on the “Program” pin must exceed the Zener diode breakdown voltage. The control logic will switch on pMOS M_0 for a short time period T_{zap} (typically several microseconds) to enable the zapping process. During this zapping process, only those Zener diodes with switched-on selection transistors will be zapped (i.e. the silicon junction is melted). After this calibration procedure, the zapped and un-zapped Zener diodes will have different resistances and so store binary information. As a result, the internal calibration settings are programmed into the chip in a non-volatile way.

4. Decision of Calibration Settings

The calibration settings (Cal , Ib , I_o , T_o , and TC) have a large impact on the transmitter performance. The values of these calibration parameters are therefore very critical. The

algorithm that determines their values works as described hereafter.

First, the on-chip current generators are made process independent. Based on the measurement result of the on-chip constant-to-temperature current and the target calibration result, one can easily calculate the required values for the process-calibration setting Cal (see Sect. 3.3 for details). The required range for the parameter Ib that sets the bias current can be derived from the possible range of the minimum VCSEL threshold. Indeed the bias current will be set by an amount ΔIb just above the minimum threshold current. The required accuracy on ΔIb is determined by the extinction ratio requirement. The maximum output power during a ‘0’ is $\Delta Ib \cdot SE_{max}$. Hence the accuracy of Ib is limited by the minimum extinction ratio requirement,

$$\frac{P_{1,min}}{\Delta Ib \cdot SE_{max}} \geq ER_{min} \quad (6)$$

where $P_{1,min}$ is the minimum output power of data ‘1,’ SE_{max} is the maximum VCSEL slope efficiency, and ER_{min} is the minimum extinction ratio requirement (i.e., 6 dB).

For the modulation current it is difficult to derive a closed-form solution due to the complexity of the piecewise linear current generation. So the values of I_o , T_o , and TC settings are determined experimentally. Light-current characteristics of VCSEL samples are measured and the required piecewise linear modulation current for a given VCSEL output power P_{out} is calculated as the following equation,

$$I_{MOD,est}(T) = I_{th}(T) + \frac{P_{out}}{SE(T)} - I_{BIAS} \quad (7)$$

where I_{th} is the threshold current and SE is the slope efficiency of the VCSELs. Then one can fit the resulting $I_{MOD,est}$ to the piece-wise linear modulation current curve by using the least squares method. Assuming the fitting curve has the deviation $d_i = I_{MOD,est}(T_i) - I_{MOD}(T_i, I_o, T_o, TC)$ for temperature point T_i , and the sum of squared error (SSE) is defined as follows,

$$\begin{aligned} SSE &= d_1^2 + d_2^2 + \dots + d_n^2 = \sum_{i=0}^n d_i^2 \\ &= \sum_{i=0}^n [I_{MOD,est}(T_i) - I_{MOD}(T_i, I_o, T_o, TC)]^2 \\ &= a \text{ minimum} \end{aligned} \quad (8)$$

Finally, the I_o , T_o , and TC settings which minimize the sum of squared error are selected for the calibration.

5. Experimental Results

The VCSEL driver was designed in a $0.6\mu\text{m}$ BiCMOS technology. Figure 10 is a microphotograph of the transmitter chip. The chip area is approximately 1.65mm^2 . The VCSEL is mounted on the metal pad in the upper right corner of the die.

The measurement setup was implemented in a chip-on-board (COB) configuration using a naked-die VCSEL. The

Fig. 10 Microphotograph of the transmitter.

Fig. 11 Output eye-diagram of VCSEL driver.

output eye diagram generated using a 50-Mb/s NRZ PRBS pattern with a length of $2^{11} - 1$ is plotted in Fig. 11. The transmitter output has a wide eye opening with a duty-cycle distortion (DCD) of +0.5% and the jitter is 1.5 ns (peak-to-peak).

The bias current is measured by applying static logic ‘0’ at the input, and the combination of bias and modulation currents is measured by applying static logic ‘1.’ Figure 12 and Fig. 13 give the bias and modulation currents as a function of temperature, as well as the measured optical output power. For three different supply voltages (3 V, 4 V, and 5.25 V), the optical output power varies within 1.1 dB over the temperature range from -40°C to 105°C and always remains below the eye-safety limit.

In addition, Fig. 14 shows the extinction ratios (ER) for different temperatures and supply voltages. The VCSEL is biased around its threshold current at room temperature. When the temperature goes to low and high extremes, the threshold current of VCSEL increases. As a result, the ER

Fig. 12 Measured bias and modulation currents versus temperature.

Fig. 13 Measured output optical power versus temperature for 3 supply voltages.

Fig. 14 Measured extinction ratio versus temperature for 3 supply voltages.

increases as well. The measurement shows that the ER is always greater than 14 dB over the whole temperature range.

6. Conclusions

A low-cost alternative optical power control scheme is proposed in this paper. Based on the proposed feedforward scheme, we have designed a VCSEL transmitter for au-

tomotive applications, in a $0.6\mu\text{m}$ BiCMOS technology. The experimental results demonstrate that the feedforward temperature compensation works very well. The optical output power varies within 1.1 dB and extinction ratio is greater than 14 dB over the temperature range from -40°C to 105°C .

References

- [1] T. Kibler, S. Pofel, G. Bock, H.P. Huber, and E. Zeeb, "Optical data buses for automotive applications," *J. Lightwave Technol.*, vol.22, no.9, pp.2184–2199, Sept. 2004.
- [2] K. Pedrotti, "High speed circuits for lightwave communications," *International Journal of High Speed Electronics and Systems*, vol.9, no.2, pp.313–346, 1998.
- [3] C. Kuznia, "Aerospace transceivers built with flip-chip VCSEL packaging," *IEEE Conference on Avionics Fiber-Optics and Photonics*, pp.39–40, 2005.
- [4] J. Ao, J. West, and E. Lamar, "Open loop thermal compensation circuit that is suitable for use in burst-mode laser transmitters," US Patent no.7054564, June 2002.
- [5] S. Odermatt, S. Eitel, M. Pfeiffer, A. Bregy, and B. Witzgmann, "Physics of VCSELs: Temperature-dependent modulation response," *Proc. 5th International Conference on Numerical Simulation of Optoelectronic Devices*, 2005.
- [6] MOST cooperation, "MOST specification of physical layer," Rev. 1.1, 2003.
- [7] A.A. Ciubotaru and J.S. Garcia, "An integrated direct-coupled 10-Gb/s driver for common-cathode VCSELs," *IEEE J. Solid-State Circuits*, vol.39, no.3, pp.426–433, March 2004.
- [8] R.J. Baker, H.W. Li, and D.E. Boyce, *CMOS Circuit Design, Layout, and Simulation*, IEEE Press, Piscataway, NJ, 1998.

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