Non-monotonic threshold voltage variation in 4H-SiC Metal-Oxide-Semiconductor Field-Effect Transistor: investigation and modeling

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Abstract— We propose an analytical model to reproduce the non-monotonic instability of the threshold voltage in 4H-SiC MOSFETs submitted to positive gate stress bias. Experimental analysis of the threshold voltage transients indicate that both electron and hole trapping take place in the gate dielectric or at the dielectric/semiconductor interface, responsible for a V_{TH} increasing-decreasing-increasing pattern. At low/moderate stress fields (<7 MV/cm), the electron trapping kinetics responsible for positive V_{TH} shift are modeled by a rate equation considering a trapping-inhibition model, that explains the logarithmic degradation kinetics. In the high field regime (>8 MV/cm), we propose that electrons can tunnel through the SiO_2 , be accelerated by the high field and generate holes through impact ionization (II) or anode hole injection (AHI). These holes are then trapped in the oxide, thus generating a negative V_{TH} shift. This second process has an exponential time-dependency, as found through the analysis of the corresponding rate equations. The time constant of the positive V_{TH} shift is evaluated as a function of stress voltage and temperature. The results indicate that the time constant is strongly dependent on the electric field (that accelerates electrons to generate holes), and not thermally activated, in agreement with theoretical considerations.

Index Terms—

I. INTRODUCTION

Silicon Carbide has excellent properties such as high thermal stability and high melting point, wide bandgap, and good bulk mobility, which make it a perfect candidate for high power and high temperature electronic devices. Compared to silicon-based devices, SiC MOSFETs provide significantly reduced static and dynamic losses, and can be used at higher frequency, temperature and power density [1]. Operation at higher frequencies with lower losses allow the fabrication of more compact, cheap and efficient power converters, inverters, Power Factor Correction circuit etc. [2-3].

Despite all these advantages, SiC MOSFETs still suffer from issues related to the gate oxide that may result in threshold voltage instabilities and/or breakdown. High defect density and metallic contamination may lead to an early oxide breakdown; thanks to optimized design and to the use of thicker gate oxides, SiC based power MOSFETs can achieve failure rates similar to Si devices

or IGBTs [4]. On the other hand, intrinsic threshold voltage instabilities are linked to the physical properties of the interfaces, such as the density of interface states, responsible for low channel inversion layer mobility [5], and border traps. Border traps are defined (*Aichinger et al* [6]) as traps within the oxide, close to SiO₂/SiC interface, where charge exchange occurs through an inelastic tunneling process, triggered by both the Fermi level position and thermodynamic energy barriers. Trapping and de-trapping kinetics at border traps may result in threshold voltage instabilities, and are still subject of intense study [6], [7],[8].

The purpose of this paper is to demonstrate a non-monotonic threshold voltage shift (ΔV_{TH}) in 4H-SiC MOSFETs subject to low and high gate electric field, and to model the related mechanisms. Specifically, i) by means of a custom setup capable of monitoring the threshold voltage variations, we test devices at different gate voltages and identify two processes responsible for the non-monotonic threshold voltage variation: a) a negative charge trapping for $\xi_{OX} < 8\text{MV/cm}$ ($V_G < 35\text{V}$), causing a positive ΔV_{TH} , b) a positive charge trapping, causing a negative shift for $\xi_{OX} > 8\text{MV/cm}$; ii) based on rate equations, we propose a model capable of reproducing the experimental data under all stress conditions. We model the positive threshold voltage shift by a self-limited electron trapping process which is temperature-independent and involves border traps; in addition, the negative V_{TH} shift is modeled by considering combined electron-tunneling, hole generation, and hole trapping in the gate insulator. The originality of our approach lies in using two differential equations in combination to model electron and hole trapping, having respectively logarithmic and exponential kinetics. Originally, we proposed a model to describe these two processes in a univocal way. Remarkably, the full model composed of the sum of the two proposed models for electrons and holes is able to reproduce the experimental data for any applied electric field. Another aspect of novelty is that this trapping-rate approach is applied on silicon carbide devices, thus providing further information on the trapping dynamics of emerging wide bandgap semiconductors. The proposed methodology can reproduce the experimental data with accuracy. iii) Finally, we study the variation of the related time constants of the hole trapping at high electric field and temperature, to validate the model and the related hypotheses.

II. EXPERIMENTAL DETAILS

The devices used in this study are lateral nMOSFET structures with gate width $W_G=2\text{ mm}$ and gate length $L_G=2\mu\text{m}$. Nitrogen-doped epi is grown in a hot- wall CVD reactor, on 6-inch Si-face 4H-SiC n+ substrates, with an off-cut angle of 4° . The p-type surface concentration is 10^{17} cm^{-3} . The gate oxide is a 40.9 nm thermally grown SiO₂, with a post oxidation nitridation to reduce interface traps. An n+ doped polysilicon gate is then deposited; the edges are covered by thick oxide layer and a metal layer is deposited as a top contact.

We developed a custom setup [9], [10], to monitor the threshold voltage variations during positive gate stress. Threshold voltage, defined as the gate voltage which correspond to a drain current of 1mA/mm, measured by means of fast (10 μs) $I_D V_{GS}$ measurements logarithmically spaced in time, ramping the gate from 0 to 10 V and keeping the drain constant at 1 V ($V_{D,pulse}=1\text{ V}$) as depicted in Fig.1. During the stress stage, a quiescent bias is applied only to the gate ($V_{G,QB}=10, 20, 30, 35, 37.5, 40\text{V}$) whereas the drain has no bias ($V_{D,QB}=0\text{ V}$).

Figure 1 – Signal sequences as a function of time applied at the gate and drain contact. Under stress conditions, $V_{D,QB}$ is kept at 0V whereas $V_{G,QB}$ is chosen according to the experiment. $V_{G,start} = 0V$ and $V_{G,STOP} = 10V$ define the 10 μs logarithmically spaced ramp to obtain the V_{TH} at 1mA/mm. $V_{G,QB}$ goes from 10 to 40 V, the duration of the stress is 100s.

III. RESULTS

Threshold voltage transients under different gate oxide stress were initially measured at 25°C. Fig.2 represents the V_{TH} shift (ΔV_{TH}) over time from 10 μs to 100 s, as a function of $V_{G,QB}$. The experimental data points are shown with symbols while a solid line is used for the model. At the early stage of the transient, V_{TH} drifts positively, independently of the applied voltage, with a logarithmic trend. This can be explained with an electron trapping at border traps located within the first few nanometers of the SiO_2 [6-7]. As long as the stress voltage V_G is lower than 30V (~ 7.5 MV/cm), electron trapping is dominant, with a constant slope throughout the stress. For the sake of simplicity, the calculated electric field does not take into account the flat-band voltage correction: $\xi_{OX} = (V_{GS} - V_{TH})/x_{ox}$ where V_{TH} is the DC threshold voltage at 1 $\mu A/mm$ and x_{ox} is the oxide thickness. At higher gate stress voltages, a second process is observed, responsible for a negative V_{TH} shift, having an exponential dependence on time, and superimposed to the original logarithmic increase. Studying the presence of positive charge in the oxide is particularly important; in fact, positive charge trapping may lead to an increase of the local electric field, accelerating the oxide breakdown, i.e. causing reliability concerns [11].

Figure 2 – Threshold Voltage drift ($V_{TH}(t) - V_{TH}(10\mu s)$) as a function of time at $T=25^\circ C$. E_{ox} is between 2.5 and 10 MV/cm. Two main behaviors can be noticed: 1) a logarithmic increase of V_{TH} due to electron trapped in the first nanometers of the SiC/SiO₂ interface, present at any stress voltage $V_{G,QB}$; 2) an exponential trapping of holes in the oxide for $\xi_{ox} > 8MV/cm$.

III.A PHYSICAL MODEL OF TRAPPING DYNAMICS

The electron trapping kinetics, detected at low/moderate fields, have a logarithmic dependence on time (see Fig. 2, $V_{GS}=10-30$ V). To model this behavior, we considered a self-limited trapping process that can be described by considering self-inhibition. This approach has been already used in literature on GaN FinFet devices [10] and it is well described in [12]. The underlying hypothesis is that once an electron is trapped, it exerts a repulsive action that inhibits trapping of further electrons in the surrounding volume (inhibition volume V_i), because of Coulombic repulsion. Hence, the capture of a single electron reduces the available traps by a factor $\left(1 - \frac{V_i}{V_{OX}}\right)$, where $V_i = \frac{4}{3}\pi \times r^3$ is the inhibition volume (of radius r), and V_{OX} is the total gate oxide volume $W_g \times L_g \times t_{ox}$.

We propose to use the following rate equation (ordinary differential equation) for the trapping rate $\frac{dn}{dt}$:

$$q \frac{dn}{dt} = A(N_T - n) \times \left(1 - \frac{V_i}{V_{OX}}\right)^n - Cn \quad (1)$$

where N_T is the total density of traps and n is the density of trapped electrons. As can be noticed, the trapping rate decreases both due to the progressively lower number of available traps ($N_T - n$), and to the increase in the inhibition volume, due to multiple trapping events, expressed by the term $\left(1 - \frac{V_i}{V_{OX}}\right)^n$.

As can be seen from the equation, for $n \ll N_T$ the density of trapped electrons increases logarithmically with time [12]-[13], thus effectively reproducing the trapping kinetics reported in Figure 2 for low stress voltages. The parameters A and C were kept constant for all electric field conditions. In (1), the term $-Cn$ considers the electrons that, under high electric field, can tunnel into the oxide reaching the metal region. Eq. (1) has been used in literature (see ref. [9]) but has never been used to describe electron trapping in 4H-SiC. With this equation we were able to extract some interesting parameters such as the inhibition radius for SiO₂/SiC border traps.

We solved the differential equation (1) numerically. We extracted as fitting parameters the inhibition radius ($r = 0.9 \text{ nm}$), and the total density of traps $N_T = 1.7 \times 10^{13} \text{ cm}^{-2}$ (which has a realistic order of magnitude). If we consider we are dealing with border traps located at position $x=x_e$ from the SiO₂/polySi interface, the magnitude of the threshold voltage shift is obtained by using Gauss' Law as explained in [14]. With $x=0$ the SiO₂/polySi interface and N_T located at x_e , the expression of the threshold voltage for electrons is

$$\Delta V_{The} = \frac{qn(t)}{\epsilon_{ox}} \times x_e \quad (2)$$

Least-square regression of the experimental data gave $x_e=39 \text{ nm}$, indicating that only the first few nm of oxide (on SiO₂/SiC side) is involved in the analyzed trapping process. This is consistent with the hypothesis of border traps formulated above.

The blue dashed straight line in Fig.3 represents the model of the positive threshold voltage shift related to electron trapping (ΔV_{The}) as a function of time. When compared to the experimental data, we see a very good fit (compare symbol and solid lines in Fig.2). A slight hole trapping is also revealed at 7.2MV/cm, however we think it can be neglected in the time window under analysis, since the hole trapping is small compared to the electron trapping. Thus, we can conclude that as long as the electric field $\xi_{ox} < 8 \text{ MV/cm}$, electrons are trapped by tunneling at the border traps located at 39 nm from the SiO₂/polySi interface. For fields higher than 8MV/cm, the electrons may tunnel by Fowler-Nordheim (FN) mechanism through the oxide without losing energy, thus being accelerated by the high field across the oxide.

Figure 3 – The Logarithmic electron trapping model responsible for positive shift ($\Delta V_{TH,e}$) and the exponential hole-trapping model responsible for the negative shift ($\Delta V_{TH,p}$), are depicted respectively in dashed blue and red, while the black straight line is the sum of the two models. As illustrated in the bottom left inset, electrons are being continuously trapped at any electric field at border traps, causing a positive threshold shift. When $\xi_{ox} > 8 \text{ MV/cm}$, the strong electric field in the oxide leads hole generation, and consequent trapping of holes in the oxide. The position of trapped holes (x_p) is also shown (see discussion below)

According to Di Maria *et al* [15] impact ionization might take place on thicker oxides for electric fields greater than 7MV/cm, while for lower values anode hole injection might occur. Their experiment is based on tests on different oxide thicknesses, and the results suggests anode hole injection occurs at high fields only on very thin oxides (less than 10nm) at the metal/oxide interface.

Using this paper as reference, we cannot exclude that in our devices, more than one mechanism can take place. Consequently, holes may be generated, either in the oxide (through impact ionization), or at the gate electrode (anode hole injection, AHI). The generated holes may tunnel back to the insulator, thus being trapped there [16] (see the bottom-left inset in Fig.3).

Holes, generated by impact ionization in the SiO₂, can be trapped in the oxide, with a certain trapping exponential dynamic (3), leading a sudden drop of V_{TH} . Holes are trapped with a uniform distribution during the injection period in a finite width layer with a center x_p as shown in the inset of Fig.3. We propose to use the following differential rate equation for describing the trapping of positive charge, previously adopted in the literature [17] for positive charge trapping on Silicon based MOS structures.

$$q \frac{dp}{dt} = J_{FN} \alpha \sigma_h \times (P_T - p) \quad (3)$$

Eq. (3) is a classic first order exponential rate kinetic that i) can precisely fit our transients and ii) is able to give some information about the hole injection probability α and the capture cross-section.

Since we consider holes to be distributed on a layer of finite thickness and considering that the negative threshold variation has exponential (and not logarithmic) kinetics, we do not consider self-inhibition for hole trapping. In (2) J_{FN} is the total DC gate current related to FN tunneling measured on the same device. α is the field-dependent hole-injection probability, taken as a fitting parameter for each voltage stress, it goes from 0.02 at 8.4MV/cm to 0.06 at 9.6MV/cm; it indicates the fraction of tunneling electrons capable of generating holes to be trapped. $\sigma_h = 1.53 \times 10^{-14} \text{ cm}^2$ represents the fitted cross sections of the hole traps in the oxide, independent of ξ_{ox} and T. Finally, P_T is the total voltage-dependent trapped positive charge. Similar to what was done for electrons, we define the equation (4) as the voltage shift caused by the hole trapping located at x_p .

$$\Delta V_{THp} = \frac{qp(t)}{\epsilon_{ox}} \times x_p \quad (4)$$

As can be understood, the closed-form solution of (4) allows to extract the product $P_T * x_p$ hence, to fit the amount of positive charge we need to fix x_p or vice versa. Based on previous reports, we suggest that the trapped holes may be stored or distributed within the insulator tunneling through the oxide. The centroid of the trapped holes can be calculated by considering that holes are trapped with uniform distribution during the stress period (as described in [17]), and by assuming that no charge trapping occurs within the electron tunneling distance f from the oxide/SiC interface. This second approach, applied to the experimental data, gives a trap centroid located 20 nm from the semiconductor interface, with a hole density of $5 \times 10^{12} \text{ cm}^{-2}$. Details on the calculations are not given here for brevity, the procedure being fully described in [17]). The dashed red curve in Fig.3 illustrates equation (4) as a function of stress time at $V_G = 37.5\text{V}$. It is worth to say that P_T may be slightly overestimated since, according to [17] the centroid shifts closer to the metal as the voltage stress increases.

At the end of hole transient, V_{TH} keeps rising due to continuous electron trapping at the border. To obtain the final model depicted with a solid line in Fig.3, the two contributions (electrons and holes) must be summed: $V_{TH} = \Delta V_{THE} + \Delta V_{THp}$. Fig.2 clearly displays that the model matches the data at any $V_{G,QB}$. As the voltage rises, the value of P_T reasonably increases; in addition, also the probability α slightly increases, as also observed by *Di Maria* [15].

III.B TEMPERATURE INFLUENCE ON THRESHOLD VOLTAGE TRANSIENTS

We repeated the experiment for a fixed $V_{G,QB}=35V$, at several temperatures to further prove the validation of our model, i.e. temperature independence of the trapping kinetics.

Figure 4 – The effective threshold voltage at 1mA/mm V_{TH} and the relative variation $\Delta V_{TH} = V_{TH}(t) - V_{TH}(10\mu s)$ are plotted at different temperatures. The latter, at the bottom side of the graph, is helpful to understand the independency of the electron trapping from the temperature hence the curves lay on top of each other in the first 10ms.

Fig.4 shows both the measured threshold voltage V_T at 1mA/mm and the corresponding threshold variation ΔV_{TH} . All measurements were collected during stress at 35 V, at different temperatures. The analysis of the V_{TH} curves at the upper part of the figure (left y-axis reference) indicates that the starting threshold voltage is decreasing with temperature. This effect is due to an increase of the channel mobility and it is well-known from both Silicon device theory [14], [18], and for 4H-SiC MOSFET [19]. Plus, the impact ionization rate hence the amount of holes generated within the oxide decreases with temperature reducing the total transient shift. The bottom region of Fig.4 depicts the threshold shift ΔV_{TH} : as can be noticed, the first phase ($t < 10$ ms) is independent of temperature. This is consistent with our model since temperature does not appear in the rate equation of electron trapping (1). With regard to hole trapping, the time constant τ , extracted from a stretched exponential fit (not shown), as a function of temperature and applied electric field is plotted in Fig.5. Although τ is almost independent of temperature (the extracted activation energy is about few meV), it has a strong exponential dependence on the electric field, i.e., a straight line on semilog plot with a slope $S = -1.66$. This observation is consistent with the idea that hole generation/trapping is initiated by the electric field across the insulator, that allows a higher amount of carriers to tunnel through the oxide, generating a greater amount of holes which, in turn, tunnel back to the oxide.

Figure 5 – Time constant as a function of temperature and electric field. The purple line shows that there is no dependency of τ on temperature. The fitted green line represents and confirms an exponential dependency of the hole trapping process at the electric fields greater than 8 MV/cm with a slope $S = -1.66$ s*cm/MV

IV. CONCLUSIONS

In conclusion, we proposed an analytical model to describe the negative charge and positive charge trapping during a fast threshold voltage transient on a SiC based MOSFET. The key-points of this work are: a) Under low constant stress, the threshold voltage increases logarithmically. The variation is perfectly described by electron trapping kinetics, by using a self-inhibition rate-equation model. Electrons trapped in the first few nanometers of the oxide are approximately $1 \times 10^{13} \text{ cm}^{-2}$. The process is found to be temperature-independent, in agreement with the proposed rate equation; b) Under high constant stress, hole trapping induces a negative shift in threshold voltage. This is modeled by considering that at high fields electrons are injected towards the gate and accelerated in the dielectric. This results in the generation of holes, that eventually are trapped in the insulator. The presented model totally matches with the experimental data, and predicts a field-dependent kinetics, with no thermal activation.

SUPPLEMENTARY MATERIAL

The author suggests seeing the supplementary material to understand the dependency of the inhibition model (1) on the total density of traps N_T and the inhibition radius r .

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Figure 1 – Signal sequences as a function of time applied at the gate and drain contact. Under stress conditions, $V_{D,QB}$ is kept at 0V whereas $V_{G,QB}$ is chosen according to the experiment. $V_{G,start} = 0V$ and $V_{G,stop} = 10V$ define the $10 \mu s$ logarithmically spaced ramp to obtain the V_{TH} at $1mA/mm$. $V_{G,QB}$ goes from 10 to 40 V, the duration of the stress is 100s.

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Figure 2 – Threshold Voltage drift ($V_{TH}(t)-V_{TH}(10\mu\text{s})$) as a function of time at $T=25^\circ\text{C}$. E_{ox} is between 2.5 and 10 MV/cm. Two main behaviors can be noticed: 1) a logarithmic increase of V_{TH} due to electron trapped in the first nanometers of the SiC/SiO₂ interface, present at any stress voltage $V_{G,QB}$; 2) an exponential trapping of holes in the oxide for $\xi_{ox} > 8\text{MV/cm}$.

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