Design of an Integrated DC-Link Structure for Reconfigurable Integrated Modular Motor Drives

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***Abstract*—In this paper, a DC-link structure feasible for integration with the circumscribing polygon modular integrated drives is proposed. The proposed DC-link structure combines both the DC-link capacitors and the bus-bar together and integrates them with the machine and the converter modules without increasing the outer diameter of the integrated machine/converter structure. A generic design methodology for the proposed DC-link structure is provided and applied on a reconfigurable fifteen stator coils concentrated winding axial flux machine for all its possible phase configurations. The design methodology presented in this paper involves the determination of the required DC-link capacitance and the multi-physics design of the bus-bar. The parasitics of the bus-bar part of the proposed DC-link structure are evaluated using electromagnetic FEM models and their influence on the DC-link waveforms is evaluated. Due to the expected high ambient temperature inside an integrated drive, electromagnetic and CFD models are developed for the proposed DC-link structure to evaluate the loss density and the temperature distribution of the bus-bar to ensure reliable operation. An experimental setup is built to validate the design methodology.**

***Index Terms*—Integrated modular drives, DC link capacitors, DC link bus-bar, Wide Bandgap converters, Parasitic inductance, Bus-bar thermal modelling, Bus-bar electromagnetic modelling, DC-link voltage spike.**

I. Introduction

INTEGRATED modular motor drives (IMMDs) represent a modularized and physically integrated machine, power converter and DC-link structure [1]. IMMDs provide the advantages of high fault tolerance and high power density compared to the conventional drives [2]- [3]. The high fault tolerance results from the redundancy and the flexibility in dividing and configuring the stator modules to maximize the torque that can be generated at a certain fault. The high power density and compactness of the drive results from the elimination of the converter separate housing and the cables connecting the converter to the machine [4].

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Many challenges have to be met for the realization of an IMMD. Among these challenges, the small space available for the converter modules has to be efficiently utilized by optimal selection of the converter components especially, the DC-link capacitor as it represents the bulkiest component in the converter module [5] beside the heatsink. One more challenge is the high thermal stresses that the converter switches and capacitors will be exposed to due to their close proximity to the major heat sources in the machine [6].

The small space and the thermal challenges of the integrated drives can be met by utilizing the wide bandgap (WBG) semiconductor devices such as the Gallium Nitride (GaN) and Silicon Carbide (SiC) in the implementation of the converter modules due to their lower losses, higher thermal conductivity, smaller package size for the same voltage and current rating compared to the Silicon (Si) devices [7]. Using WBG devices makes it possible to switch with higher frequency than the Si case which results in smaller DC-link capacitance [8].

IMMDs are classified according to the location of the power converter modules with respect to the machine housing and the stator elements into: axially stator iron mounted (ASM), radially stator iron mounted (RSM), axially housing mounted (AHM), radially housing mounted (RHM) [9] and circumscribing polygon (CP) integration topology [10]. The RSM, ASM and CP provide a more compact integrated drive with higher cooling design challenges.

In this paper, a DC-link structure feasible for physical integration with CP modular integrated drives is proposed. This DC-link structure combines both the capacitors and the bus-bar. Besides the possibility of the physical integration with the integrated machine/converter structure, the proposed DC-link structure in this paper provides four more advantages. The first one is that the proposed DC-link structure doesn't increase the outer diameter of the integrated machine/converter structure which results in a more compact integrated structure. The second one is that it has a small parasitic inductance from the capacitor terminals to the converter DC input terminals which reduces the voltage spike on the converter switches. The third one is that it has a relatively high inductance from the DC-source input terminals to the capacitor terminals which further smooths the current supplied from the DC-source reducing the electrical and the thermal stresses on it. The fourth one is that the bus-bar part is easy to manufacture and the capacitors are chosen off the shelf and no need for the time consuming and the expensive custom designed DC-link structure as proposed in [11].

The authors in [5]- [12]- [13] address the design of the

DC-link capacitor for three phase drives with a single set of stator winding. The authors in [14]- [15] handle the influence of the pulse width modulation (PWM) carriers interleaving on the design of the capacitor of the three phase drives with dual stator winding. In [16], the authors illustrated the possibility of using carrier interleaving with IMMDs but no closed form generic design equations are given. In [**?**], the authors presented generic analytical design equations for the DC-link capacitors of the reconfigurable IMMDs. These equations are adopted in this paper.

The DC-link bus-bar connects the DC-source, the capacitors and the converter modules together [17]. In [18]- [19]- [20]- [21], the authors study the influence of the bus-bar geometry for three phase inverters implemented using commercial half-bridge modules on the value of the parasitic inductance. Lacking in literature, a comprehensive study for an integrated bus-bar structure feasible for IMMDs given their special structure and high ambient temperature.

In this study, a generic design methodology for the proposed DC-link structure feasible for reconfigurable modular integrated drives is provided and applied on a fifteen stator coils circumscribing polygon integrated axial flux drive. The design process presented in this paper involves the determination of the required DC-link capacitance for each configuration and the multi-physics design of the bus-bar. An electromagnetic FEM model and CFD model are developed for the proposed DC-link structure to ensure that the electrical and the thermal stresses on the components of the DC-link structure are within the rated values.

The electromagnetic FEM model is used to extract the DC-link structure parasitics so that, the DC-link voltage spike can be estimated, and to compute the loss density distribution in the bus-bar. This loss density distribution is used as an input to a CFD model for the DC-link structure to compute the temperature distribution. In this way, both the electrical and the thermal stresses on the bus-bar can be evaluated to ensure reliable operation in the high ambient temperature environment of the integrated drive.

The paper is organized as follows: section II provides a brief description of the CP integrated drive for which the DC-link structure is designed and analysed. In section III, the mechanical construction of the proposed DC-link structure is explained. Section IV discusses in detail the design of the proposed DC-link structure. The experimental setup and results are given in section V and then the conclusion is given in section VI.

II. Structure of the CP IMMD

The integrated DC-link structure proposed in this paper is applied on an IMMD with fifteen stator coils with circumscribing polycon integration of the power converter modules [10]. Fig. 1 shows the construction of this CP integrated drive. The drive combines the electric machine, the power converter modules, the shared cooling structure and the DC-link structure. The polygon shaped shared cooling structure with the converter modules mounted on top is illustrated in Fig. 2. Table I contains the main specifications of this integrated drive topology.

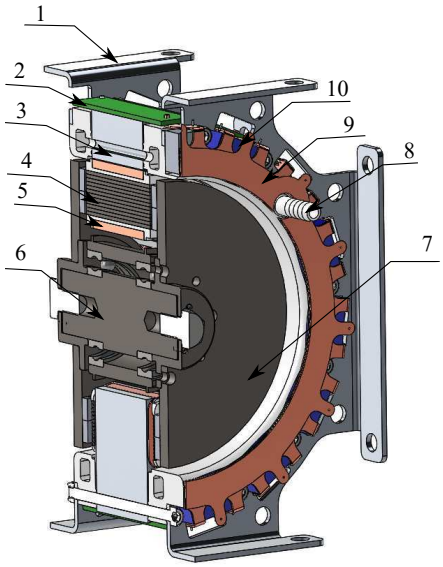

Fig. 1. A CP integrated drive: (1) Mounting structure, (2) Converter module PCB, (3) Cooling channel, (4) Core, (5) Winding, (6) Shaft, (7) Rotor disc, (8) Cooling fluid fitting, (9) DC-link bus-bar, (10) DC-link capacitor

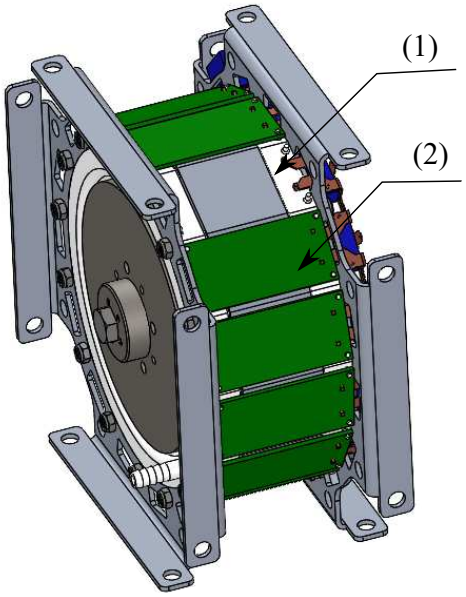

Fig. 2. The polygon shaped shared cooling structure with the converter PCB on top: (1) The polygon shared cooling structure, (2) Converter module PCB

Each converter module has a size of 60×40 mm^2 and is capable of providing up to 1.13 kW. The converter is implemented using GaN technology. Fig. 3 shows a picture for the implemented GaN based half-bridge module.

III. Mechanical construction of the integrated DC-link

Fig. 4 shows the construction of the proposed DC-link structure. It consists of a ring shaped bus-bar with the DC-link capacitors arranged circumferentially pointing radially inward. In this way, the bus-bar and the capacitors are integrated with

TABLE I
THE KEY SPECIFICATIONS OF THE INTEGRATED DRIVE

Quantity	Value
rated power (kW)	17
rated speed (rpm)	2500
# pole pairs	8
# slots	15
axial length (mm)	60
outer diameter (mm)	190
converter module size (mm^2)	60×40

Fig. 3. The GaN based half-bridge module

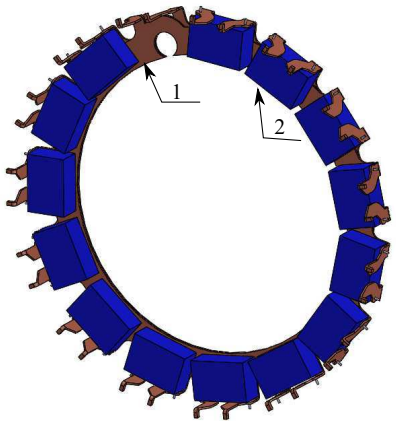

Fig. 4. The DC-link structure: (1) The bus-bar structure, (2) The DC-link capacitors

the machine/converter structure without increasing the outer diameter which enhances the compactness of the drive.

Fig. 5 shows an exploded view for the bus-bar part of the DC-link structure. It consists of a positive plate, a negative plate and an electrical insulation layer between them. Each plate has an input tab for the DC-source, a connection terminal for the module capacitor and a connection terminal for the converter input source. A short distance of 17.5 mm between the capacitor terminal and the converter DC-input terminal is achieved which results in a small AC parasitic inductance and hence small switches voltage spike. A relatively longer average distance of 115 mm between the DC-source input tab and the converter input terminal is achieved which results in a relatively greater DC parasitic inductance and hence a smoother DC-source current and smaller DC-source stress will result.

The conducting plates can be made of copper or aluminium.

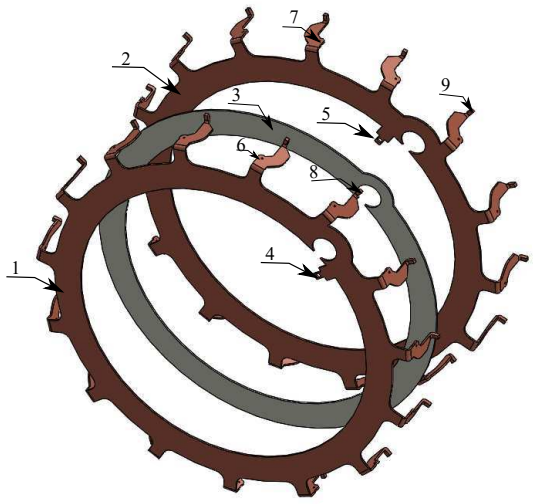

Fig. 5. DC-link bus-bar structure for a modular fifteen stator coils drive: (1) Positive plate, (2) negative plate, (3) insulation layer, (4) DC-input plus, (5) DC-input minus, (6) capacitor plus terminal, (7) capacitor minus terminal, (8) converter module plus input, (9) converter module minus input

TABLE II
PROPERTIES OF INSULATION MATERIALS

Material	E (kV/mm)	ϵ_r	rated temperature (°C)	K_{th} (W/m.K)
Kapton	196	3.7	400	0.4
Mylar	295	3.3	105	0.14
Nomex	17-33	1.6	220	0.157
FR4	49	4.3	140	0.31

Using aluminium plates results in a lighter drive due to the smaller mass density of aluminium compared to copper but higher loss and temperature will result due to the smaller electrical and thermal conductivity of the aluminium. The insulation layer can be made of kapton, mylar, nomex or epoxy glass (FR4). Table II contains the main properties of the insulation materials. Here, E is the breakdown strength, ϵ_r is the relative permittivity and K_{th} is the thermal conductivity. As the maximum bus-bar temperature is limited by the rated temperature of the insulation layer, kapton represents the optimal choice from the thermal point of view.

IV. DESIGN OF THE DC-LINK STRUCTURE

The design of the integrated DC-link structure involves the determination of the DC-link capacitors for each possible configuration of the modular drive and the multi-physics analysis of the mechanical outline of the integrated bus-bar part of the DC-link structure.

A. Selection of the DC-link capacitors

By proper DC-link voltage scaling and stator coils connection, the fifteen stator coils of the integrated drive in Fig. 1 can be configured to operate as three phase, five phase or fifteen phase drive [**?**]. In case of three phase operation, five stator coils are connected in series to form one phase as in Fig. 6.

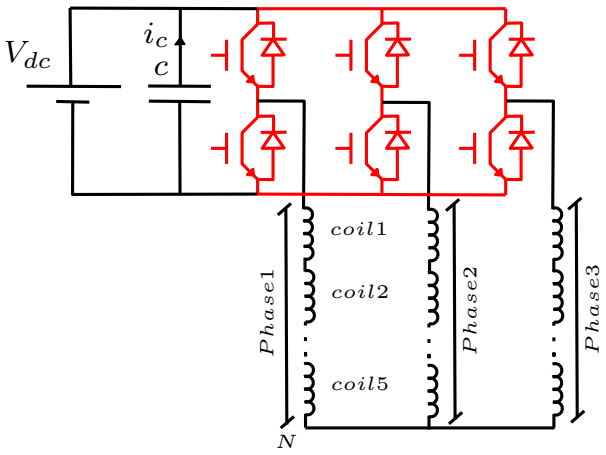

Fig. 6. The connection in case of three phase operation

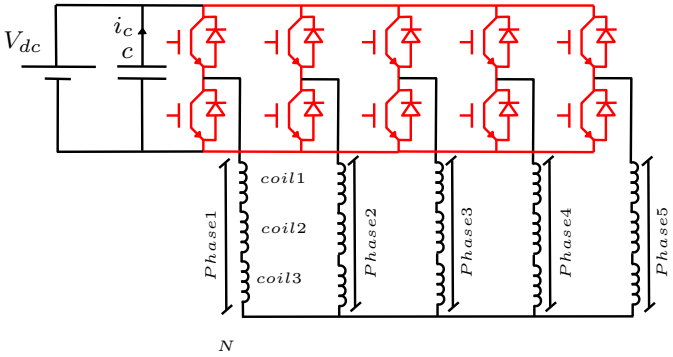

Fig. 7. The connection in case of five phase operation

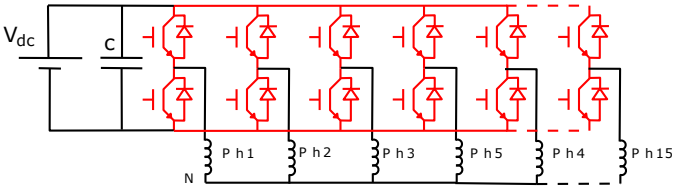

Fig. 8. The connection in case of fifteen phase operation with one common neutral

In case of five phase operation, three coils are in connected in series to form one phase as in Fig. 7. In case of fifteen phase operation, the stator coils can be connected to have one common neutral point as in Fig. 8, divided into five groups with three coils in each group as in Fig. 9 or divided into three groups with five coils in each group as in Fig. 10. For the connections in Fig. 9 and Fig. 10, the pulse width modulation carriers can be shifted by an interleaving angle K to further reduce the DC-link current stress. Each configuration has its own Torque-speed and fault-tolerance characteristics.

Equations (1), (2) can be used to calculate the DC-link capacitor harmonic currents while (3) and (4) can be used to estimate the value of the needed DC-link capacitance [**?**]. The equations are valid for each possible configuration of the reconfigurable modular drives. The DC-link capacitance requirement of the reconfigurable drive in Fig. 1 is calculated for each configuration considering 400 V DC-link voltage in case

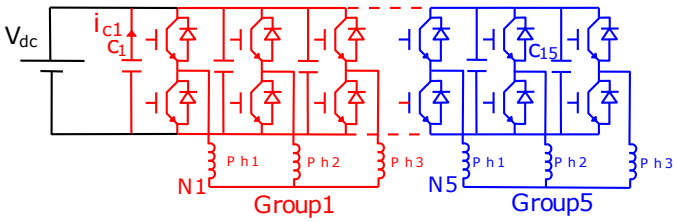

Fig. 9. The connection in case of fifteen phase divided as five groups with three phase in each group

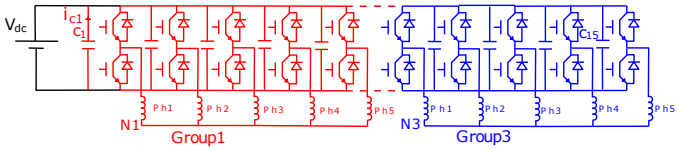

Fig. 10. The connection in case of fifteen phase divided as three groups with five phase in each group

of three phase operation. For the other configurations, the DC-link voltage is adjusted to keep the phase current and power the same. The design is performed for 1% $V_{ppripple}$. Table III contains the calculated DC-link capacitance requirements per module for each configuration.

$$i_{ch}(n,m) = \frac{i_{linepeak}}{2\pi^2} \sum_{s=1}^{g} \sum_{h=1}^{N} \int_{y_{min}}^{y_{max}} f(x,y) dy dx \quad (1)$$

$$\begin{cases} f(x,y) & = \cos(x - \phi + n\theta) e^{i(my+nx)} \\ y_{min} & = \frac{\pi}{2}(1 - M\cos(x + n\theta)) + K \\ y_{max} & = \frac{\pi}{2}(3 + M\cos(x + n\theta)) + K \end{cases} \quad (2)$$

$$C_{min} = \frac{I_{mde}}{\pi f_{md} V_{ppripple}} \quad (3)$$

$$I_{mde} = \sqrt{\sum_{n=-\infty}^{\infty} I_{ch}^2(n, m_{md})} \quad (4)$$

where, $i_{ch}(n,m)$ is the capacitor's peak harmonic current at harmonic order (m) and its side-bands (n) around the inverter output fundamental frequency f_o, $i_{linepeak}$ is the peak output current of the inverter, g is the number of groups, N is the number of phases, ϕ is the phase shift between the fundamental output voltage and the fundamental output current of the inverter, θ is the electrical phase shift between the phases, K is the interleaving angle, $m_{md} = \frac{f_{md}}{f_s}$ is the harmonic order of the capacitor's most dominant harmonic current component, f_s is the switching frequency, f_{md} is the frequency of the capacitor's most dominant harmonic current component, I_{mde} is the capacitor's equivalent most dominant harmonic current, $V_{ppripple}$ is the peak to peak capacitor ripple voltage, C_{min} is the minimum required DC-link capacitance.

The film capacitor FB27A6J0335 from AVX with the specifications in Table IV is selected for the capacitor module.

As the ambient temperature inside an integrated drive is expected to be high, the calculation of the capacitor power

TABLE III
DC-LINK CAPACITOR REQUIREMENTS FOR EACH PHASE CONNECTION

Variable	Connection	Value
Minimum rated voltage (V)	3-ϕ	400
	5-ϕ	240
	15-ϕ	80
	5×3-ϕ	80
	3×5-ϕ	80
Minimum ripple current rating (A)	3-ϕ	1.92
	5-ϕ	1.8
	15-ϕ	1.75
	5×3-ϕ	0.3
	3×5-ϕ	0.4
Minimum capacitance (μF)	3-ϕ	2
	5-ϕ	3.2
	15-ϕ	9.5
	5×3-ϕ	0.5
	3×5-ϕ	0.65

TABLE IV
KEY SPECIFICATIONS OF THE SELECTED CAPACITOR MODULE

Variable	Value
rated voltage (V)	550
rated rms ripple current (A)	5
capacitance (μF)	3.3
ESR (mΩ)	22
$\tan(\delta)$	2e-4
thermal resistance R_{th} (°C/W)	27.3
rated hotspot temperature (°C)	100
ESL (nH)	25

loss and hot spot temperature is crucial. (5) can be used to calculate the power loss and the hot spot temperature of the capacitor. The worst case module capacitor loss is calculated to be 0.0814 W which means a temperature rise of 2.3 °C above the ambient. Note that this small loss results thanks to the modular construction of the drive that divides the DC-link current ripple over the capacitor modules.

$$\begin{cases} P_d & = \frac{1}{2} C \tan(\delta) \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} V_{pph}^2 f_h \\ P_t & = \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} I_{chrms}^2(n,m) \times \\ & \quad ESR(n,m) \\ \theta_{hotspot} & = \theta_{ambient} + (P_d + P_t) R_{th} \end{cases} \quad (5)$$

Here, C is the value of the selected capacitance, $\tan(\delta)$ is the dielectric loss tangent, V_{pph} is the peak to peak ripple voltage resulting from the harmonic with frequency (f_h), I_{chrms} is the harmonic current rms value for one module capacitor, ESR is the equivalent series resistance at the harmonic (n,m), P_d is the dielectric loss component, P_t is the loss in the ESR, $\theta_{ambient}$ is the maximum allowable ambient temperature, $\theta_{hotspot}$ is the maximum allowable capacitor hotspot temperature, R_{th} is the maximum thermal resistance of the capacitor from its hotspot to the ambient. C,$\tan(\delta)$,R_{th},ESR are all extracted from the datasheet of the selected capacitor.

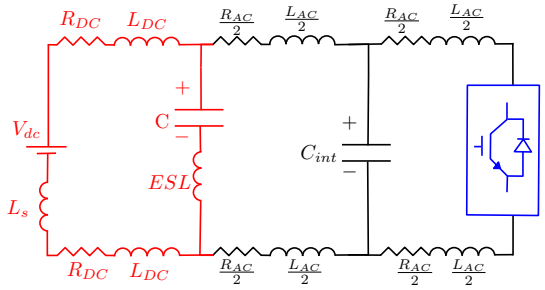

Fig. 11. Per module bus-bar equivalent circuit

B. Electromagnetic analysis of the bus-bar

The electromagnetic analysis is performed for two purposes. The first one is to evaluate the DC-link parasitics [17] so that, the electrical stresses over the bus-bar insulation and the converter switches can be evaluated. The second one is to evaluate the electromagnetic loss density distribution over the bus-bar due to the DC and the AC currents so that, the temperature distribution over the bus-bar can be evaluated.

1) Bus-bar parasitics and electrical stresses: Fig. 11 shows the per module equivalent circuit of the DC-link structure in Fig. 4. The values of the parasitic components of the DC-link structure are computed using electromagnetic FEM and listed in Table V as per module values. The values are computed for 1 mm thick copper and aluminium plates considering a 1 mm Kapton insulation layer. L_{AC} is the plate parasitic inductance from the capacitor terminals to the converter module input terminals. L_{AC} and ESL constitute a part of the commutation loop inductance.

Due to the high transition speed of the GaN switches [9], any small parasitic inductance in the commutation loop contributes considerably to the voltage stress on the switches and the bus-bar insulation during turn-off transition of the switches. The switch voltage spike above the DC-link voltage can be estimated from (6). To illustrate the influence of the parasitics on the module terminals voltage stress, the circuit in Fig. 11 is simulated considering the three phase configuration of the drive and the dynamic model of the GaN switch GS66508B used in the implementation of the converter. Fig. 12 (left) shows the resulted converter module terminal voltage, a spike of 73 V above the 400 V DC voltage can be observed. Since the peak voltage is 473 V, this can still be tolerated by the switches and the bus-bar insulation.

$$\begin{cases} V_{spike} & = L_{loop} \frac{di_a}{dt} \\ L_{loop} & = 2L_{AC} + ESL + L_{PCB} \end{cases} \quad (6)$$

where, V_{spike} is the switch spike voltage, i_a is the transistor current during commutation, L_{PCB} is the PCB inductance.

The influence of adding four 0.1 μF ceramic capacitors close to the terminals of the converter module is shown in Fig. 12

TABLE V
PER MODULE BUS-BAR PARASITIC VALUES

Plate material	Parameter	Value
Copper	$R_{DC}(m\Omega)$	1.125
	$L_{DC}(nH)$	409
	$R_{AC}(m\Omega)$	0.3
	$L_{AC}(nH)$	16.04
	$C_{int}(pF)$	36.08
Aluminium	$R_{DC}(m\Omega)$	1.725
	$L_{DC}(nH)$	409
	$R_{AC}(m\Omega)$	0.3
	$L_{AC}(nH)$	16.04
	$C_{int}(pF)$	36.08

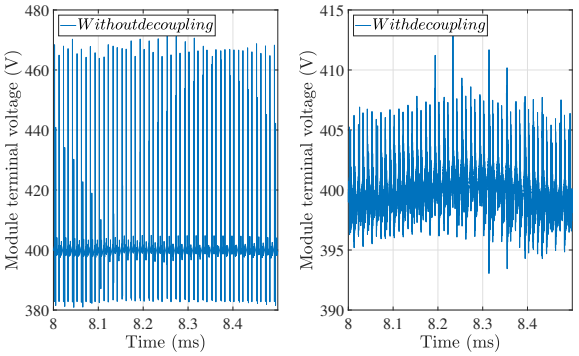

Fig. 12. The module terminal voltage spike due to the DC-link parasitics (left) and spike reduction by decoupling (right)

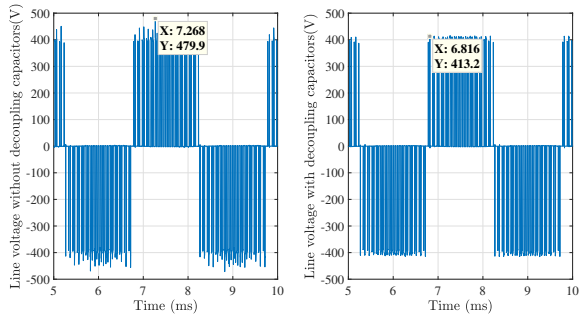

Fig. 13. The line voltage spike due to the DC-link parasitics (left) and spike reduction by decoupling (right)

(right). The additional capacitors reduce the voltage spike to 12 V.

The effect of the parasitics on the line voltage with and without the decoupling capacitors is evaluated and reported in Fig. 13. It can be seen that the effect on the DC-link voltage waveform is directly reflected on the line voltage.

The effect of the parasitics on the phase voltage with and without the decoupling capacitors is evaluated and reported in Fig. 14. A smaller influence on the phase voltage spike can be noticed as it is affected by the transient switching behaviour of only one inverter leg. The decoupling capacitors are reducing the phase voltage spike by about 23V.

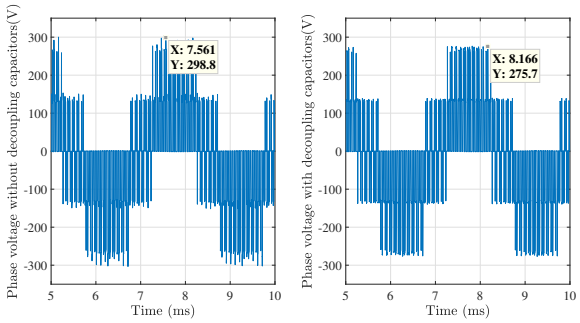

Fig. 14. The phase voltage spike due to the DC-link parasitics (left) and spike reduction by decoupling (right)

L_{DC}, computed as the total DC inductance seen between the DC input terminals multiplied by the number of modules, smooths the DC-source current which reduces the electrical and the thermal stresses on the DC-source. Note that the L_{DC} is 25 times higher than L_{AC} which is an advantage for the proposed DC-link structure. C_{int} is the capacitance between the plates and it further smooths the inverter terminal voltage. R_{AC} and R_{DC} cause the power loss and the temperature rise of the bus-bar.

2) Bus-bar loss density distribution: The highest bus-bar loss occurs for the fifteen phase configuration with common neutral point due to the lowest DC-link voltage and the highest capacitor current. The loss in the bus-bar occurs due to the DC and the AC currents drawn from the DC-source and the capacitors. The DC-current (I_{dc}) is computed from (7) considering 90% efficiency (η) and the AC-current is computed from (4). The values of the DC and the AC currents are 236 A and 35 A respectively.

$$I_{dc} = \frac{P_r}{\eta V_{dc}} \tag{7}$$

where, P_r is the rated drive power, V_{dc} is the DC-link voltage.

Both the AC and the DC current are injected in the bus-bar and the loss density is evaluated in case of copper plates (Fig. 15) and aluminium plates (Fig. 16). It can be seen that the maximum loss density is located at the input DC tabs due to the higher DC current compared to the AC one and also the total DC-current of the fifteen modules is passing through the input tabs unlike the AC current that divides over the fifteen capacitors. The maximum loss density is 1.53 times higher in case of aluminium plates compared to copper plates due to the lower electrical conductivity of the aluminium.

C. CFD analysis of the bus-bar

A CFD model is built to evaluate the temperature of the bus-bar components to ensure that the insulation temperature is below its rated value given the high ambient temperature inside an integrated drive. Assuming an ambient temperature of 50°C, natural air convection and the loss density distribution in Figs. 15 and 16, the temperature field is evaluated and shown in Figs. 17 and 18 for the plates and the insulation layer in case of copper and aluminium plates respectively. The thermal properties of the materials used in the simulation are

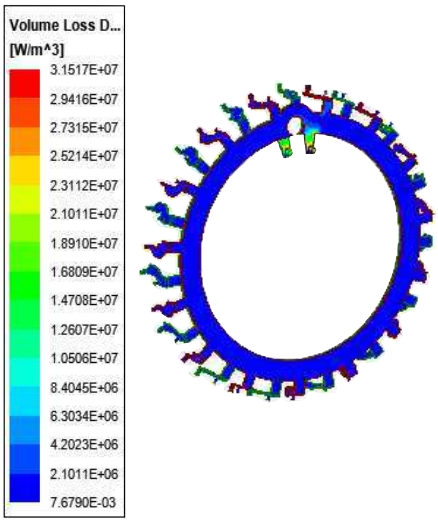

Fig. 15. The bus-bar loss density distribution due to the AC and the DC current in case of copper plates

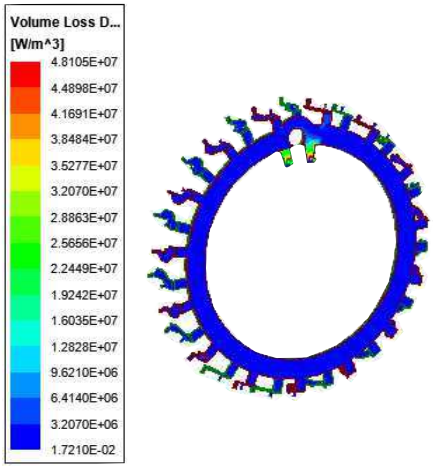

Fig. 16. The bus-bar loss density distribution due to the AC and the DC current in case of Aluminium plates

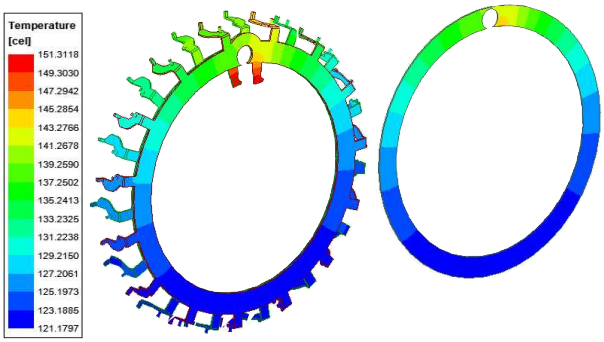

Fig. 17. The bus-bar temperature distribution in case of copper plates with plate temperature (left) and insulation temperature (right)

given in Table VI. Here, ρ and C_p are the mass density and the specific heat capacity respectively.

The insulation temperature rises 97.3°C and 165.8°C above the ambient for the copper and the aluminium plates respectively. For both materials, the insulation temperature stays

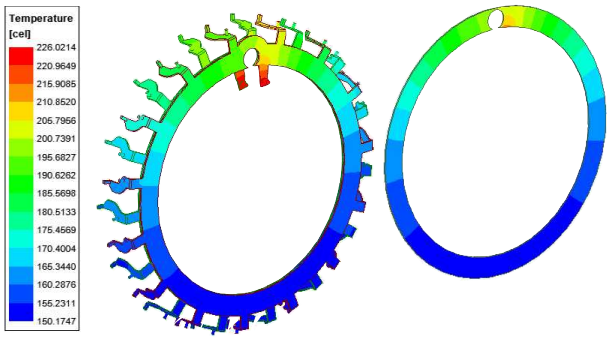

Fig. 18. The bus-bar temperature distribution in case of aluminium plates with plate temperature (left) and insulation temperature (right)

TABLE VI
THERMAL PROPERTIES OF THE BUS-BAR MATERIALS

Material	K_{th} (W/m.K)	ρ (kg/m^3)	C_p (J/kg.K)
Copper	385	8890	392
Aluminium	167	2712	896
Kapton	0.4	1330	1420

below the rated value of the Kapton material. The 68.5°C more temperature rise in case of aluminium plates is due to the higher loss density and the lower thermal conductivity of the aluminium. It can be seen also the higher temperature gradient in case of aluminium plates due to the lower thermal conductivity. The maximum insulation temperature is 15% and 28.5% higher than the average in case of copper and aluminium plates respectively.

V. EXPERIMENTAL RESULTS

The three teeth integrated setup shown in Fig. 19 is built to validate the design concepts. It consists of three GaN converter modules (Fig. 3), three stator teeth, an $R = 11.5\Omega, L = 3$ mH load and a DC-link PCB. The line currents are measured with the on board current sensor ACHS-7123 while the capacitor currents are measured using the current probe TCPA300 with the static transfer function of 10 A/mV. All waveforms are visualized using a Tektronix 1 GHz bandwidth scope. The sinusoidal PWM technique is utilized and the control pulses are generated using the dSPACE MicroLabBox. The three modules are operated as three phase inverter.

The capacitor current is measured at switching frequency 10 kHz, fundamental frequency of 50 Hz, and three different peak line currents of 7.5 A, 5.5 A and 3.8 A to compare the measured rms value with the calculated value (4). With the value of the RL load used and 50 Hz, the resulting power factor is 0.997 near to unity to evaluate the worst case value [13]. Fig. 20 shows the measured three phase line currents in case of 7.5 A peak.

The capacitor current at 7.5A peak line current is shown in Fig. 21 for ten power cycles and Fig. 22 for ten switching cycles. The measured and the calculated capacitor rms current at different peak line currents are reported in Table VII with the percentage error between them.

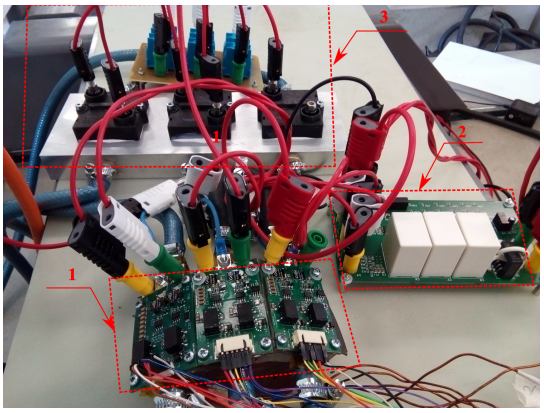

Fig. 19. Experimental setup: (1) The three teeth, (2) The DC link board, (3) The Load

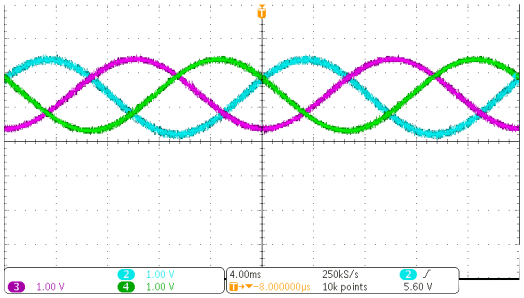

Fig. 20. The three phase currents with 7.5A peak

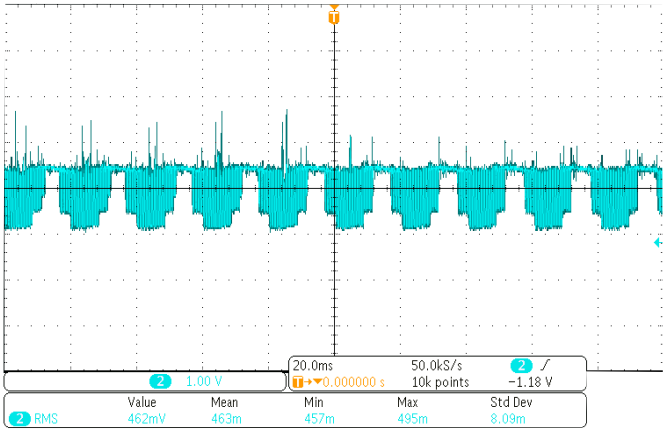

Fig. 21. The capacitor current for 10-power cycles

TABLE VII
CAPACITOR MEASURED AND CALCULATED RMS CURRENT

Peak line current (A)	capacitor rms current		% error
	measured	calculated	
7.5	4.62	4.35	-5.7
5.5	3.41	3.2	-6.1
3.8	2.48	2.35	-5.3

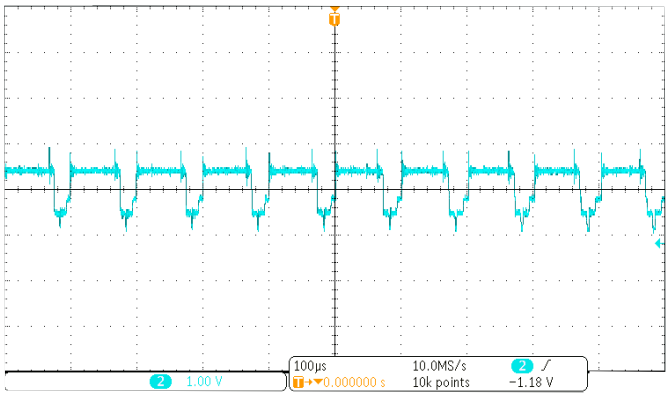

Fig. 22. The capacitor current for 10-switching cycles

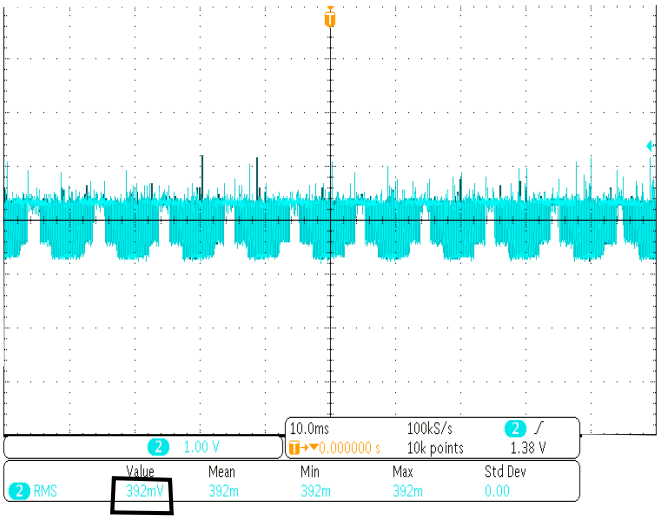

Fig. 23. The capacitor current at 10kHz switching frequency

The difference between the measured and the calculated current is mainly resulting from the influence of the parasitics and the decoupling capacitors.

The influence of the switching frequency on the capacitor current is visualized by measuring the capacitor current at a constant peak line current of 6.5 A and two different switching frequencies (10 kHz, 30 kHz). Fig. 23 shows the measured capacitor current at 10 kHz and Fig. 24 at 30 kHz with the rms value marked on the graph. A 20.6% increase in the capacitor rms current can be observed at 10 kHz. The reason of the decrease of the capacitor current with the increase in the switching frequency is the higher inductive impedance of the DC-link that further smooths the current at the higher switching frequency.

The estimation of the capacitor power loss using (5) is assessed by measuring the capacitor temperature at two different line currents (5.5 A, 3.8 A) and comparing the thermally measured power with the electrically calculated power. Both measurements are captured at ambient temperature of 25°C and free air convection. The capacitor is covered with a black tape for a better emissivity and temperature measurement accuracy. The resulted hot spot temperature is 36.7°C and 34.1°C for 5.5 A and 3.8 A peak line current respectively.

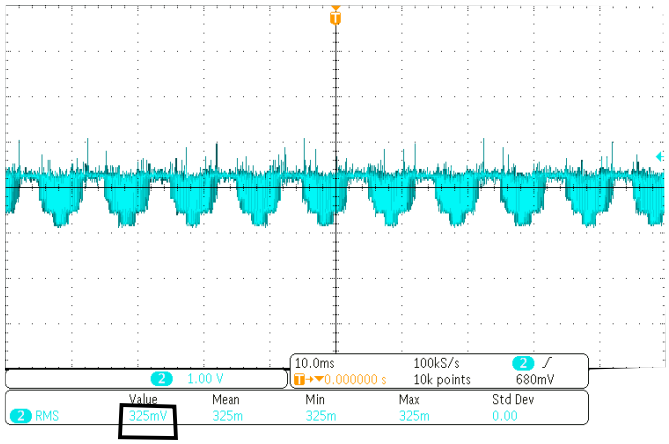

Fig. 24. The capacitor current at 30kHz switching frequency

TABLE VIII
CAPACITOR MEASURED AND CALCULATED LOSSES

Peak line current (A)	capacitor loss		% error
	measured	calculated	
5.5	0.508	0.594	16.9
3.8	0.3957	0.464	17.2

Table VIII contains the capacitor power loss measured thermally and calculated electrically with the percentage difference between both of them. The difference between the measurements and the calculations can be explained as follows: The variation of the ESR and the thermal resistance of the capacitors with temperature is not given in the datasheet of the selected part instead, fixed values at 25°C are given. Neglecting the variation of these parameters with temperature introduces an error in the calculation of the capacitor losses. The capacitor temperature is measured with the thermal camera (GTC 400), the measured value has an error of 3°C, this represents the measurement error. Since the measured capacitor temperature is less than 37°C, the contribution of the thermal camera measurement error is expected to be the main reason of the discrepancy.

Fig. 25 shows the manufactured DC-link bus-bar installed on the stator of the integrated drive shown in Fig. 1. The bus-bar is manufactured from Aluminium of 1mm thickness. The thermal performance of the bus-bar is tested by injecting 55A (to limit the temperature of the wires connecting the DC-source to the bus-bar) in the DC-input tabs at ambient temperature of 25°C and the resulted temperature distribution is reported in Fig. 26. At such current, the bus-bar hot spot at the input tabs reaches 110°C much smaller than the rated value of the Kapton, an indication of the possibility to inject higher input current.

VI. Conclusion

An integrated DC-link structure topology for reconfigurable modular motor drives is proposed and extensively analysed in this paper. The proposed topology has many advantages for the reconfigurable modular integrated drives. It combines both the

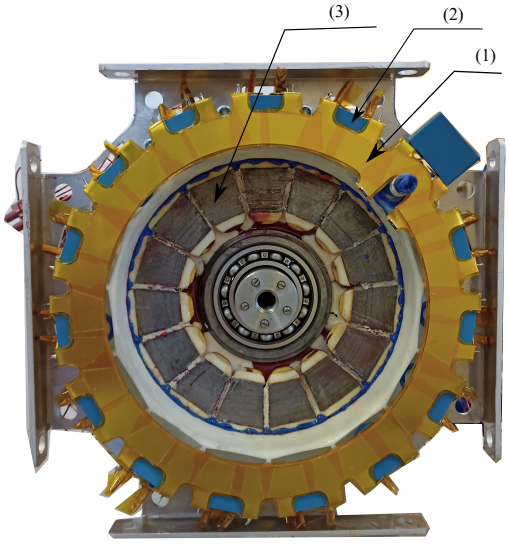

Fig. 25. The manufactured stator of the integrated drive with the bus-bar installed: (1) the DC-link bus-bar, (2) the DC-link capacitor, (3) the stator teeth

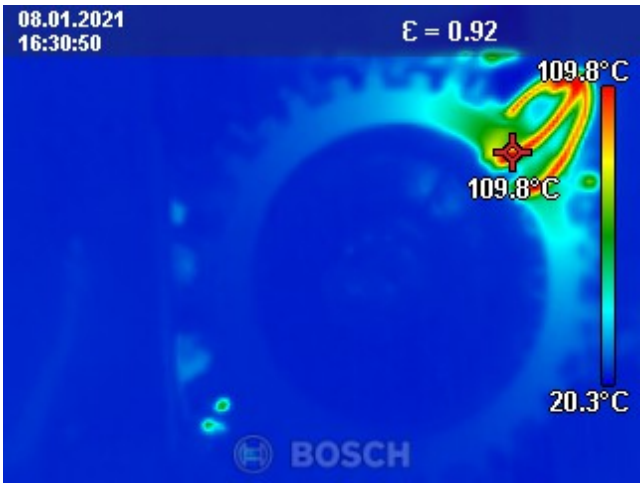

Fig. 26. The temperature distribution over the bus-bar measured at 55 A input DC-current

capacitors and the bus-bar together and integrates them with the modular integrated converter/machine structure without increasing the outer diameter of the integrated converter/machine set which enhances the compactness of the integrated drive. The per module AC parasitic inductance from the capacitor terminals to the inverter input terminals is calculated to be 16 nH which is a small value compared to the ESL resulting in a small voltage stress on the switches. The per module DC parasitic inductance is also calculated to be 409 nH which is a relatively high value resulting in a smoother DC-link current and hence, lower thermal stresses on the DC-source.

The proposed DC-link structure is designed for a fifteen phase reconfigurable circumscribing polygon integrated drive for all its possible configurations. Generic analytical equations for the design of the DC-link capacitors for any configuration are provided. Considering the high ambient temperature inside the integrated drive, the electromagnetic loss density distribu-

tion of the bus-bar is computed and supplied to a CFD model to compute the bus-bar temperature. The calculated temperature is proven to be tolerable by the bus-bar components.

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