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Threshold Voltage Instability Mechanisms in p-GaN Gate AlGaN/GaN HEMTs

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***Abstract*—In this study, we propose a technique to evaluate the transient threshold voltage behavior of p-GaN capped AlGaN/GaN high-electron-mobility transistors (HEMTs). The threshold voltage is monitored from 10 μs to 100 s during positive gate bias stress. Technology computer-aided design (TCAD) simulations offer in-depth analysis of the different threshold voltage instability mechanisms: (i) electron trapping at the AlGaN/GaN interface, (ii) hole accumulation and trapping at the p-GaN/AlGaN interface and in the AlGaN barrier, respectively, and (iii) hole depletion of the p-GaN layer.**

I. Introduction

Gallium nitride (GaN) high-electron-mobility transistors (HEMTs) show great promise in high power applications, as a result of their high breakdown field and the existence of a two-dimensional electron gas (2-DEG), yielding a high electron sheet density and mobility [1]. Additionally, they can be used at higher switching frequency compared to traditional Si power devices [2]. Normally-OFF operation is desired in many power applications due to fail-safe operation and for improving the slew rate with direct control of the gate of the AlGaN/GaN device [3]. Local p-type GaN capping of the barrier results in positive threshold voltages. It is shown that ON-state operation induces a threshold voltage shift [4], [5], which could result in a significant operation point drift, degrading the power efficiency. Threshold voltage instabilities in p-GaN gated AlGaN/GaN HEMTs have been reported in [6], [7], [8]. In this study, we present a technique to evaluate the threshold voltage under on-state gate stress. Additionally, the resulting threshold voltage transients are explained using technology computer-aided design (TCAD) simulations.

II. Device and Stress Procedure Description

The devices under test in this study are normally-off p-GaN capped AlGaN/GaN HEMTs ($W = 200\,\mu$m), on 6 inch GaN-on-Si wafers. The gate region is capped with a p-type doped GaN layer, on which a Schottky contact is formed. Initially, the enhancement mode device is characterized using a more standardized double pulse measurement setup [5]. A novel testing procedure is established to monitor the threshold voltage of the device during positive gate bias stress, schematically represented in Fig. 1. Before each measurement cycle, the device is kept at zero bias on all terminals for 100 s to promote de-trapping. During the 'stress' phase, a positive gate bias is applied during a window of 10 μs to 100 s. The stressing phase is interrupted by a very short (10 μs) gate voltage sweep in order to monitor the threshold voltage (at $I_D = 10\,\mathrm{mA/mm}$) as a function of time.

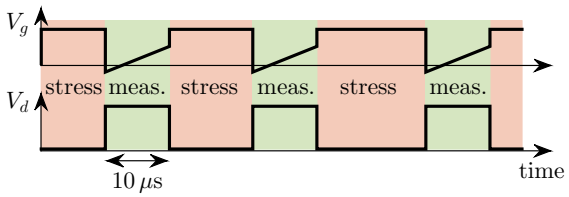

Fig. 1. Schematic representation of the gate and drain voltage during the threshold voltage transient measurement. The 'stress' and 'measurement' phase are shown in red and green, respectively.

III. Results

The initial double pulse characterization is depicted in Fig. 2, using an ON-state stressing phase of 100 μs and measurement phase of 1 μs. Pulsed $I_D V_G$ measurements at $V_D = 3\,\mathrm{V}$ in Fig. 2(a) show a positive threshold voltage shift for gate voltages up to 2 V, after which the shift becomes

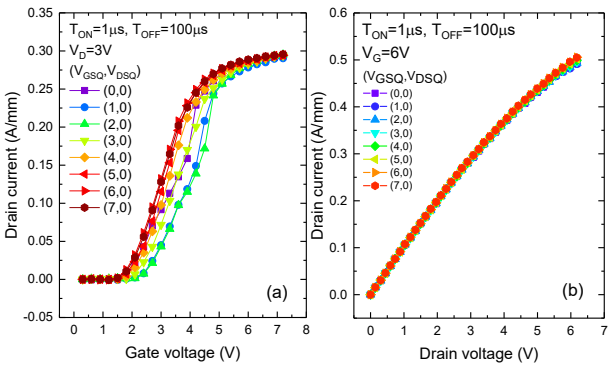

Fig. 2. Double pulse measurements showing the drain current versus (a) gate voltage at $V_D = 3\,\mathrm{V}$ and (b) drain voltage at $V_G = 6\,\mathrm{V}$. No degradation in ON-resistance is observed, indicating that the trapping phenomena are concentrated under the gate region. The stress and measurement pulse last 100 and 1 μs, respectively.

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negative and saturates at $V_G = 5\,\mathrm{V}$. The pulsed $\mathrm{I_D V_D}$ characteristic at $V_G = 6\,\mathrm{V}$ is depicted in Fig. 2(b), showing no ON-resistance shift after ON-state stress. From this, we conclude that the trapping phenomena responsible for the threshold voltage shift are located solely in the gate region.

Under the measurement conditions depicted in Fig. 1, the threshold voltage can be monitored as a function of stress time. The experimental threshold voltage is plotted in Fig. 3(a) for gate stress voltages ranging from 1 to 7 V. Note that in order to study the physical mechanisms behind the threshold voltage transients, the former is normalized w.r.t. its value at 10^{-5} s, represented in Fig. 3(b). Three major threshold voltage variation mechanisms can be distinguished, and we propose the following phenomena at its origin:

(i) electron trapping at the AlGaN/GaN interface, yielding a positive ΔV_{th} shift at low gate bias [4-6];

(ii) hole accumulation at the p-GaN/AlGaN interface and subsequent hole trapping in the AlGaN barrier [7], yielding a negative ΔV_{th} shift which appears at lower stress times with increasing gate bias;

(iii) hole depletion by forward biasing of the p-i-n diode [7], leaving behind a net negatively charged p-GaN layer, resulting in a slow, positive ΔV_{th} shift at high gate bias.

Each mechanism will be investigated in more detail in Section IV. While subject to different stress timings, both the double pulse and the threshold voltage transient measurement show similar threshold voltage behavior, where the latter shifts positive at low gate bias, and becomes negative at higher gate bias.

The temperature dependence of the V_{th} variation transient at $V_G = 2\,\mathrm{V}$ and 5 V is investigated in Fig. 4(a)-(b), respectively, in which the threshold voltage variation is plotted between 30 °C to 130 °C. At low gate bias, electron trapping causes a positive threshold voltage variation. Note that due to the

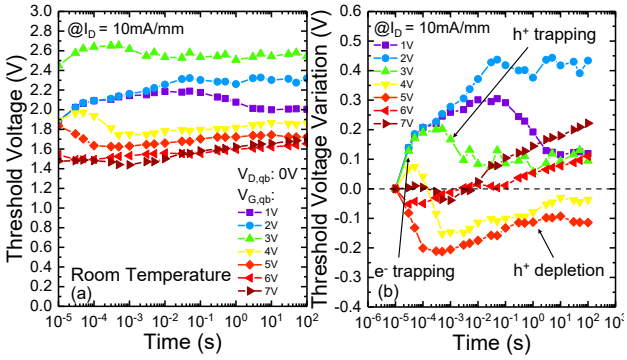

Fig. 3. Experimental (a) threshold voltage and (b) threshold voltage variation versus stress time for gate stress voltages from 1 to 7 V at room temperature. The threshold voltage is extracted at $I_D = 10\,\mathrm{mA/mm}$. Three distinct sets of slopes can be distinguished: (i) a fast positive slope due to electron trapping at the AlGaN/GaN interface, (ii) a fast negative slope due to hole trapping in the AlGaN barrier, and (iii) a slow positive slope due to hole depletion after the p-i-n diode has turned on. All effects show similar slopes, irrespective of gate bias.

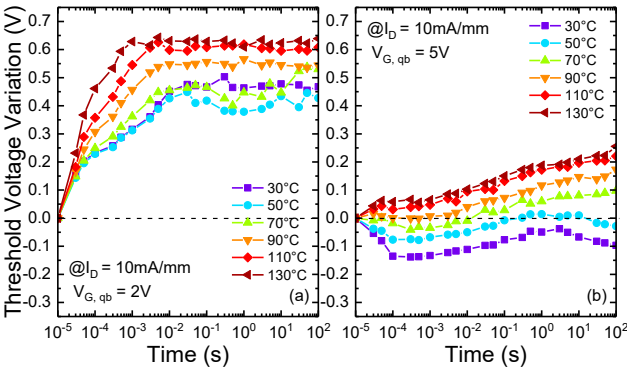

Fig. 4. Experimental threshold voltage variation versus stress time at different temperatures for (a) $V_G = 2\,\mathrm{V}$ and (b) $V_G = 5\,\mathrm{V}$.

presence of the 2-DEG at $V_G = 2\,\mathrm{V}$ the AlGaN/GaN interface states are filled with electrons. On the other hand, with increasing temperature, thermally excited 2-DEG electrons can be trapped in trap states within the AlGaN barrier, resulting in an increase of the total negative charge density in the AlGaN barrier and consequently the threshold voltage variation (see Section IV-A). At higher gate bias, a higher hole current density is injected across the Schottky barrier at the gate contact, resulting in higher rate of hole accumulation and trapping. Consequently, the fast negative slope shifts to time constants below 10^{-5} s, rendering them invisible on this plot.

IV. Discussion

Fig. 5 depicts the threshold voltage variation extracted from TCAD simulations in the case of a low (Fig. 5(a)) and high (Fig. 5(b)) level of leakage through the p-GaN/AlGaN/GaN barrier. In case (a), similar trends compared to Fig. 3 are seen, i.e. (i) a fast positive slope due to electron trapping at the AlGaN/GaN interface, and (ii) a fast negative slope due to hole trapping in the AlGaN barrier. Both electron and hole trapping saturate when the available states are filled. Only when the p-

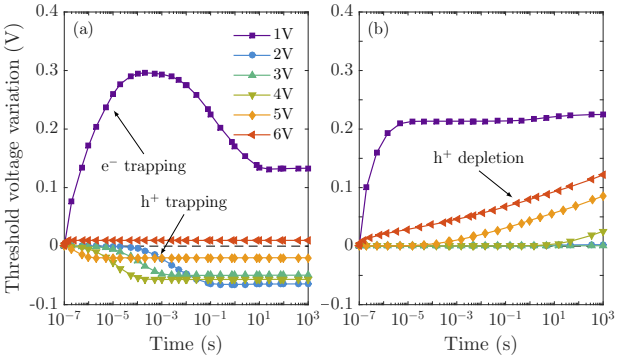

Fig. 5. Threshold voltage variation extracted from TCAD simulations at room temperature in the case of (a) low and (b) high p-i-n diode leakage level. Both cases are simulated with a highly conducting Schottky gate.

i-n leakage level is increased in the TCAD simulations (case b) a slow positive slope due to hole depletion (iii) is observed. In this case, holes recombine with electrons from the 2-DEG and the p-GaN layer is partially depleted of holes, resulting in a net negative charge and hence a positive threshold shift. Saturation of this effect occurs at a much later point in time. In reality, this effect can occur as a band-to-band recombination process within the AlGaN barrier, or recombination as a result of local low-field electron injection over the AlGaN barrier into the p-GaN layer, through dislocation lines or Al clusters in the former [9]. The threshold voltage variation is calculated during positive gate bias stress using the surface potential ψ_s according to [7], so as not to interfere with the stressing phase. The three threshold voltage shift mechanisms are investigated using TCAD simulations and are shown schematically on the energy band diagram of the gate stack in Fig. 9.

A. Electron Trapping

At positive gate stress voltages, electrons within the 2-DEG are injected in acceptor-like interface states at the AlGaN/GaN interface. The capture time constant depends on the density of available electrons, hence a function of the gate voltage. Fig. 6 shows the threshold voltage variation versus stress time at $V_G = 1\,\mathrm{V}$ for three different values of interface traps at the AlGaN/GaN interface. With increasing trap density, more electrons are trapped at the interface during the positive gate stress, yielding a positive threshold voltage variation. This is reflected in the interface electron density shown on the right axis of Fig. 6. As soon as all available trap states are filled with electrons from the 2-DEG, the effect saturates. The apparent shift in time constant with increasing interface trap density is a result of the increased gate capacitance. With increasing temperature, electrons are trapped in the AlGaN barrier, causing a further positive increase of the threshold voltage. At $10^{-1}\,\mathrm{s}$, however, the effect of hole accumulation

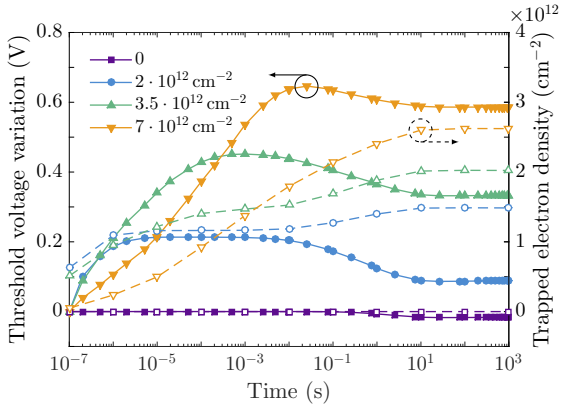

Fig. 6. Left axis: threshold voltage variation versus stress time at $V_G = 1\,\mathrm{V}$ for increasing interface trap density at the AlGaN/GaN interface. These states are uniformly distributed between 0.05 and 0.65 eV below the conduction band. Right axis: interface trapped electron density at the AlGaN/GaN interface versus stress time.

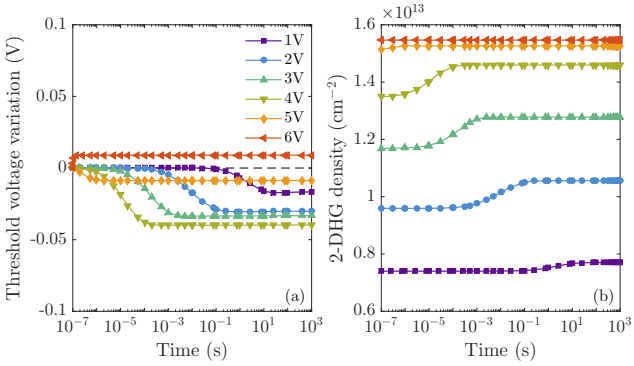

Fig. 7. (a) Simulated threshold voltage variation versus stress time without acceptor traps at the AlGaN/GaN interface. (b) Hole density in the 2-DHG versus stress time for different ON-state stress voltages.

(see Section IV-B) can be observed, yielding a negative V_{th} shift. This is accompanied by an increase in the 2-DEG density and subsequent interface trapped electron density.

B. Hole Accumulation/Trapping

Fig. 7(a) shows the simulated V_{th} transients without acceptor traps at the AlGaN/GaN interface. In this case, the electron trapping as discussed in Section IV-A is absent. Fig. 7(b) shows the two-dimensional hole gas (2-DHG) density (located at the p-GaN/AlGaN interface) versus stress time for different gate stress voltages. The time constant in the V_{th} transient corresponds to an accumulation of holes in the 2-DHG, caused by the release of holes trapped in Mg acceptor states and resulting in a slight increase in the depletion region width. This accumulation of holes at the p-GaN/AlGaN interface, both temperature and gate voltage accelerated, yields an initial negative V_{th} shift. Additionally, some of these holes are injected into Mg acceptor states in the AlGaN barrier, which are ionized at equilibrium [10]. The range of hole trapping into Mg trap states, and hence the charge distribution in the

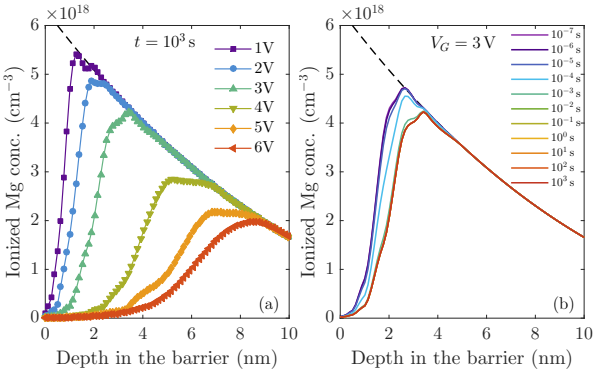

Fig. 8. Simulated ionized Mg charge density versus depth in the barrier, relative to the p-GaN/AlGaN interface, (a) for different gate bias at $t = 10^3$ s, and (b) for different stress time at $V_G = 3\,\mathrm{V}$. The Mg out-diffusion tail is represented in black dashed line.

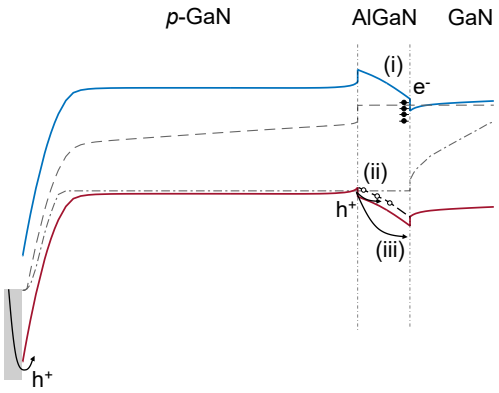

Fig. 9. Energy band diagram of the Schottky metal/p-GaN/AlGaN/GaN gate stack at $V_G = 6\,\mathrm{V}$ with three different threshold voltage variation mechanisms.

barrier is both gate bias and stress time dependent, as can be seen in Fig. 8. With increasing gate bias and stress time, more holes are injected from the Schottky contact through thermionic field emission [11] and consequently over the AlGaN barrier towards the channel. As a result, negatively charged Mg acceptor states in the barrier are neutralized by hole trapping, reducing the total equilibrium charge density and yielding a negative threshold voltage shift, according to [10]. At a fixed gate bias, the trap occupation is time dependent and saturates after a certain stress time.

C. Hole Depletion

At high gate bias, the p-GaN potential is such that the p-i-n diode is forward biased. Holes are emitted from the p-GaN layer into the GaN channel, leaving behind a net negatively charged p-GaN layer. In contrast, electrons injected from the channel into the p-GaN quickly recombine with the high density of available holes in the 2-DHG. In TCAD, this can be simulated by increasing the leakage through the p-i-n diode. The resulting threshold voltage transients are shown in Fig. 5(b). By introducing a trap-assisted-tunneling path in the AlGaN barrier, the 2-DHG accumulation supplied by the Schottky contact or extension of the depletion region is inhibited. As such, the hole accumulation and subsequent trapping discussed in Section IV-B is absent and a positive threshold voltage shift is observed. Note that the slope of the V_{th} transients at high gate bias are constant.

Comparing the TCAD predicted V_{th} transients presented in Fig. 5 to the experimental results in Fig. 3(b), we can comment that in order to obtain all three mechanisms at once, a delicate balance in leakage levels between the Schottky and p-i-n diode is necessary. In reality, this leakage can occur in local 1-D spots, whereas the 2-D simulator assumes an ideal gate stack across the complete width of the device.

V. Conclusion

In this study, we propose a measurement procedure to investigate the threshold voltage during positive gate bias stress in p-GaN capped HEMTs from $10\,\mu\mathrm{s}$ to $100\,\mathrm{s}$. TCAD simulations provide unique insight in the different mechanisms causing the threshold voltage instability. (i) At all gate positive biases, electron trapping occurs in interface states at the AlGaN/GaN heterojunction interface. (ii) At medium gate voltages, hole injection occurs at the Schottky junction which accumulate at the p-GaN/AlGaN interface, resulting in an enhancement of the 2-DHG. Subsequently, hole trapping occurs in Mg acceptor states located at around $150\,\mathrm{meV}$ above the valence band in the AlGaN barrier. (iii) At high gate bias, the p-GaN potential is high enough to forward bias the p-i-n diode, resulting in injection of holes from the p-GaN layer into the GaN channel. Similarly, electron injection occurs in the opposite direction, and these electrons quickly recombine with the high concentration of holes in the 2-DHG. Both effects result in depletion of holes in the p-GaN layer, yielding a positive threshold voltage shift.

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