Fast timing measurement for CMS RPC Phase-II upgrade

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ABSTRACT: With the increase of the LHC luminosity foreseen in the coming years, many detectors currently used in the different LHC experiments will be dramatically impacted and some need to be replaced or upgraded. The new ones should be capable to provide time information to reduce the data ambiguity due to the expected high pileup. We propose to equip CMS high-|\eta| muon chambers with pairs of single gap RPC detectors read out by long pickup strips PCB. The precise time measurement (< 150 ps) of the signal induced by particles crossing the detector on both ends of each strip will give an accurate measurement of the position of the incoming particle along the strip. The absolute time measurement, determined by RPC signal (around 1.5 ns) will also reduce the data ambiguity due to the highly expected pileup and help to identify Heavy Stable Charged Particles (HSCP).

The development of a specific electronic chain (analog front-end ASIC, time-to-digital converter stage and printed circuit board design) and the corresponding first results on prototype chambers are presented.

KEYWORDS: Data acquisition circuits; Front-end electronics for detector readout; Resistive-plate chambers
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1 The CMS RPC system phase-II upgrade

The CMS muon RPC upgrade at high rapidity ($\eta$) region extends the geometrical acceptance of the RPCs from $|\eta| = 1.9$ to 2.4, as described in CMS muon TDR [1]. We propose to equip the new rings RE3/1 and RE4/1 with improved RPCs (iRPC) which can handle high rates (figure 1).

Figure 1. R-z cross section of a quadrant of the CMS detector, including the Phase-II upgrade RE3/1 and RE4/1, designed as iRPC and shown in purple. The interaction point is at the lower left corner [1].

– 1 –
Installation of RE3/1 and RE3/1 is motivated by the following reasons:

- The RE3/1 and RE4/1 chambers extend the current $\eta$ coverage of CMS muon system at high $\eta$ and increase redundancy in this particular region.

- The intrinsic time resolution of the new RE3/1 and RE4/1 chambers improves background hits and low $p_T$ tracks rejection. It also helps to resolve ambiguities in the endcap trigger for multiple tracks identification and allows for example the reconstruction of a hypothetical slowly moving Heavy Stable Charged Particles (HSCP) [2].

Each ring is divided in 18 cassettes, each of them covering an active area of $20^\circ$ in azimuth. Inside each cassette, one large readout Printed Circuit Board (PCB) covers the active area of two bakelite RPC detectors (1.4 mm bakelite plates and 1.4 mm gas gap) covering both faces of the PCB. The readout PCB consists of 96 trapezoidal strips whose length is the total active area length of the iRPC. Each end of each strip is connected to one channel input of the Front-End Board (FEB), having in total 192 readout channels per cassette.

The resolution in the radial direction is driven by the width of readout strips whereas resolution along the strip is given by the differential measurement of time of arrival of both signals generated by one detected particle in the RPC detectors and travelling along the strip towards the readout electronics.

2 Readout printed circuit board (PCB) design

2.1 Technological constraints

The readout PCB design is driven by two main constraints:

- The first one is linked to PCB manufacturing technology. The large size of the detector lowers a lot the number of companies able to manufacture such a device. Moreover, it further requires a very simple cross section (basically no internal connections between layers). We developed two solutions to accommodate technological constraints with detector needs. For the first one, called coaxial design, strips are connected to FEB input channels using coaxial cables with the same impedance as the strip inside the cassette. For the second one, called return design, return strips are embedded in the PCB itself (with controlled impedance at the same value as the strip impedance inside the cassette) and a single connector is used to send signals up to the FEB. In both cases, strips are designed as the central layer of the PCB with a $300 \mu$m FR4 insulator on both sides. For the return version an additional local ground plane is placed on top and bottom layers. (figure 2 and figure 3).

- The second one is linked to signal propagation along the strip. In order to avoid signal reflections, it is important to keep control of the impedance of the chain from strip to the FEB input.

Resistivity of the high voltage graphite conductive layers of the RPC detector is too high for these layers to behave as the ground reference for the transmission line and does not define the strip
Figure 2. Cross section perpendicular to the strips of the coaxial (left) and return (right) versions of the readout PCB. FR4 insulation layer is in green and copper (pick-up strips, return strips and ground planes) are in orange.

Figure 3. View of the coaxial (left) and return (right) versions of the readout PCB. Dimensions are in mm.

Figure 4. Schematic view of longitudinal structure of the mechanical cassette, detector and readout PCB (cassette in blue, insulation layer in red, RPC detector in yellow, PCB in green and pick-up strips in orange).

We can define strip impedance as shown in eq. (2.1). Four parameters define the strip impedance:

\[ Z_C = \sqrt{\frac{R_S + jL_S \omega}{G_P + jC_P \omega}} \quad (2.1) \]
Geometrical dimensions of the strips and strip material define the ohmic resistance $R_S$ value that describe the ohmic losses along the transmission line conductor. Strip dimensions are function of the number of channels on each detector (96), width and length of the RPC detector active area. Strips material is defined by the manufacturing process (copper). Then strip impedance $L_S$ is also defined similarly by the strips material and strip geometry. The dielectric capacitance $C_P$ is defined by the dielectric thickness (RPC detector and FR4) and material. The dielectric conductance $G_P$, describing losses in the dielectric part of the transmission line is also defined by iRPC and FR4 thickness and material.

In order to maximize charge transfer between the RPC detector and strip, we must minimize thickness of the FR4 layers of the PCB to reduce distance between strips and conductive layers of the gaps. Considering the large size of the PCB, 300 $\mu$m of FR4 on each side of the strips seems to be the minimal acceptable value in terms of mechanical rigidity and handling capabilities. Therefore, the only way to adjust strip impedance is by modifying the distance between the strips and the mechanical ground plane of the cassette.

In case of the coaxial version of the system, we must use this to accommodate the available impedance of coaxial cables compliant with the system in terms of external diameter. Whereas in case of the return version, we must carefully measure the impedance of the strips to define the geometry of the return strips to match impedance of the return strips (defined by respect to the local ground planes) to the impedance of the pick-up strip.

### 2.2 Impedance experimental measurement

After the coaxial strip PCB has been installed inside a cassette between two iRPC detectors, we first simulated the impedance of the whole set using a simulation tool. But, due to limited knowledge of the RPC detector dielectric permeability, this can be only used as a rough estimation of the strip impedance. Therefore, we applied three experimental methods to measure the strip impedance.

The first one consists in measuring separately each line parameter ($R_S$, $L_S$, $C_P$ and $G_P$) with a RLC meter (Quadtech 7600). $R_S$ and $L_S$ are measured while shorting the end of the line to ground while $C_P$ and $G_P$ are measured with and opened line. The second one (load matching) is made by injecting a pulse at one side of the strip and adjusting a variable load at the other side of the strip to suppress reflections. The third one (reflective) is based on behaviour of a non adapted line at the very first instants of an injected pulse where the line behaves as if it was an ohmic resistor whose value is its characteristic impedance of the line.

All these methods lead to the results given in table 1. Measurements were made for both sides of the strips giving similar results. Knowing this we define the impedance value for return strip of the second version of the readout PCB as 44 $\Omega$. It is interesting to notice that in case of a lossless transmission line, $G_P$ and $R_S$ are negligible and the line impedance is then defined only by $L_S$ and $C_P$. In our case, although $R_S$ is small and could be neglected due to the wide geometry of the strips, $G_P$ can not be neglected (because of intrinsic structure of the RPC detector itself).

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1TNT Transmission line electromagnetic simulation tool suite version 1.2.2. [https://sourceforge.net/projects/mmtl/files/](https://sourceforge.net/projects/mmtl/files/)
Table 1. Simulated and experimental measurement of strip impedance in cassette for the coaxial prototype.

<table>
<thead>
<tr>
<th></th>
<th>Simulation</th>
<th>Direct measurement</th>
<th>Termination matching</th>
<th>Reflective method</th>
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</thead>
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<td>$R_s$ (mΩ)</td>
<td>160</td>
<td>461</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$L_s$ (nH)</td>
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<td>487</td>
<td>Not available</td>
<td>Not available</td>
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<tr>
<td>$G_p$ (µS)</td>
<td>0</td>
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<td>$C_p$ (pF)</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>$Z_c$ (Ω)</td>
<td>51</td>
<td>44</td>
<td>46</td>
<td>41</td>
</tr>
</tbody>
</table>

3 Front-end board design

The prototype front-end board is based on two main components: a fast front-end ASIC and a time-to-digital converter. The front-end ASIC is called PETIROC [3], it is a 32 channels version developed in SiGe technology. It hosts a preamplifier with a 1 GHz bandwidth and gain of 25 associated with a fast programmable comparator (figure 5). Overall jitter of PETIROC is kept at 20 ps for an input charge of 300 fC. Threshold and pedestal alignments of the 32 channels are made by individually adjusting internal DAC for both pedestal and comparator level.

![Figure 5](image)

**Figure 5.** Schematic view of the PETIROC ASIC. Used parts of the ASIC in this design are showed between red lines and unused parts are greyed.

The output of the comparator for each PETIROC channel is fed into an Altera cyclone II FPGA hosting the time-to-digital (TDC) conversion module. This TDC, called wave union [4], is based on a set of identical delays whose each output is connected to a latch stage. The input signal is propagated across the delay chain and on each rising edge of the system clock, value of output of each delay is frozen and, knowing the individual propagation delay of cells, the state of each delay cell output gives access to the global delay between the incoming signal and the edge of the clock. A coarse clock counter completes time measurement by respect to an acquisition window or
a common start signal. In this system quantification step is given by the propagation delay of one delay element (around 20 ps for a carry element inside a cyclone II FPGA).

Inside a standard FPGA, logic elements are organized in Logic Array Blocks (LAB) and even if delay between two elements inside one LAB is small and well known, due to routing constraints inside the FPGA, the delay between elements of separated LABs can be of the same order of magnitude as one delay element of the chain. This problem is solved in the wave union TDC by generating two consecutive edges for each input signal and wisely separating them to ensure that at any time at least one of those signals is not located between two LABs.

The FEB, in its prototype version, embeds logic to synchronize with other Front-end boards (common clock, common acquisition window, synchronous trigger and reset). A TCP-IP processor (Wiznet W5300) is also added to receive commands, set ASIC configuration parameters and send acquisition data to the DAQ PC.

4 System electrical tests and behaviour

It is important to have all channels of the PETIROC ASIC aligned to the same pedestal value to check good behaviour and a coherent response of each channel. We perform this procedure in three separated stages. Each time, the threshold of the comparator is lowered step by step with a short acquisition window and output data are recorded.

First, with only one channel activated at once in the PETIROC ASIC, we obtain data used to align all channels pedestal DAC values. Those data are individually saved in a configuration database. Then, with all channels activated together but no readout board connected to the PETIROC inputs, the same procedure is applied in order to check alignment computed in the first step. Lastly, with all channels activated together and the readout board connected to the FEB, we can check alignment and hunt for system noises or grounding issues. An example of alignment results is given in figure 6.

![Figure 6](image)

**Figure 6.** Alignment results for one standard front-end with only the FEB (left) and FEB and readout board (right). For each curve, inflexion point is fitted to an error function (erf).

In order to validate the good behaviour of the PETIROC ASIC in his environment, we performed a linear scan of injected charges between 200 fC and 500 fC on each side of the readout board with mechanical cassette and RPC detectors. Results are shown in figure 7. We obtain a linear response.
of 0.18 ADC count per fC in the dynamic range between 200 fC and 500 fC. If we consider the pedestal to be at the y-intercept of the linear fit (464 DAC counts) and with the programmed threshold value (494 DAC counts), we can estimate the minimum charge that can be seen in this system to 152 fC for the readout strip. As the signal splits toward both ends of the pickup strip, it corresponds to 76 fC per PETIROC input.

![Figure 7](image.png)

**Figure 7.** Linearity scan with injection of a known charge for high (left) and low (right) radius of one strip of coaxial type readout board. Charge is generated with a square pulse generator and a 1 pF serial capacitor and threshold is set to 494 DAC counts.

Finally, in order to determine the efficiency of the system with respect to the injected charge, we perform a scan of several injection pulse levels through a 1 pF capacitor (injection is located on one side of the readout board). Corresponding results are shown in figure 8. Efficiency plateau is reached on injection side at 180 fC and 200 fC on the other side. This situation is the worst case that can be observed: in this case, there is no attenuation on the injected side, all charge is transferred to the PETIROC input whereas the signal arriving at the other side has seen attenuation of the whole readout strip. With this level of injection, the time obtained resolution is around 200 ps, which corresponds (with the propagation speed of signals in the pickup strip of \( \approx 18 \) cm/ns) to a spatial resolution along the strip of 3.6 cm.

## 5 Conclusion

Longitudinal position along a pickup strip measurement by using the difference of time of arrival of signal has been proven to be possible with a good spatial resolution. Same measurement campaign has to be repeated for the return type prototype in order to evaluate its performances and freeze the final design.

There are still several improvement possibilities in order to gain in precision and in sensitivity. A new version of the PETIROC ASIC is under study with an adjustment of the gain versus bandwidth to reach lower threshold. Implementation of Time-over-Threshold (ToT) in the TDC will allow both to estimate the input charge and compensate time-walk on the input signal.
Figure 8. Efficiency (8A) and time resolution (8B) measured versus charge injected on low radius of the readout board. Injection side (red points) and opposite side (blue points).
References


