Challenges for Designing Large-scale Integrated Photonics

Wim BOGAERTS [1,2*]
[1]Ghent University – IMEC, 9000 Ghent , Belgium
[2]Luceda Photonics, 9200 Dendermonde, Belgium
[*] wim.bogaerts@ugent.be

With the growing adoption of silicon photonics in data- and telecommunication as well as sensing and spectroscopy, the difficulties of designing larger circuits in this technology have become more prominent. Silicon photonic waveguides have submicron dimensions, and can therefore be integrated in large numbers on a chip. But these same submicron dimensions give rise to extreme sensitivity of the waveguide response to small variations in geometry, temperature, stress etc. Multiply this with thousands of functional building blocks and even more interconnects, and it is clear that it becomes very challenging to guarantee the correct functionality of a photonic integrated circuit. Even if the circuit is nominally correct, compound variability can still dramatically lower the yield.

When designing silicon photonic chips, it is important to start from a workflow which has the largest chance of transferring the intent of the designer to a working chip layout for fabrication. Such a workflow is known in electronic design automation (EDA). It makes sense to reuse this model from electronics because photonic circuits are ever more tightly integrated with electronics, both technologies make use of similar planar manufacturing processes, design frameworks exist and there is a large community of expertise. An EDA workflow starts from a schematic circuit that can be optimized for the desired functionality. As electronics and photonics use different physics, it is challenge is to combine the two circuit models into a single design flow. The circuit description can then be implemented in a chip layout manually or with assistance of a *schematic driven layout* tool. Again, photonics imposes different constraints on layout than electronics. The resulting layout should then be verified against design rules (*design rule check*) and the functionality is checked against the original specifications (*layout-vs-schematic*). Here as well, photonics imposes challenges in extracting the connectivity and verifying the curved geometries.

While the similarities in design flows already enable photonic designers to a large extent, the challenges in each step, combined with the inherent variability of the process and operational conditions, make it very hard to accurately predict the yield of larger circuits. *Design-for-Manufacturability* (DfM) techniques that are used for electronics cannot necessarily be applied for photonics. We will discuss the different challenges in detail and also present some of the solutions that are emerging.

[1] W. Bogaerts, M. Fiers, P. Dumon,, *Design Challenges in Silicon Photonics*, J. Sel. Top. Quantum Electron., vol. 20, no. 4, 1-8, 2014
[2] L. Alloatti, M. Wade, V. Stojanovic, M. Popovic and R. J. Ram, *Photonics design tool for advanced CMOS nodes,* in IET Optoelectronics, vol. 9, no. 4, pp. 163-167, 8 2015.
[3] M. Heins, et al. *Design Flow Automation for Silicon Photonics: Challenges, Collaboration, and Standardization,* Silicon Photonics III. Springer Berlin Heidelberg, 2016. 99-156.