Poly-Ge/poly-CdSe thin-film circuits for on-glass integrated driving of flat-panel displays

**English Summary**

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Processing .......................................................................................................... 25

Most of the work, but not much to say about.

Evaluation (see chapter 6) ................................................................................. 25

The realised devices and circuits will be evaluated in several ways.

Chapter 2 : Technology design .................................................................................................................. 27

2.1 Introduction .............................................................................................................. .............. 27

The existing technology for CTFT circuits ................................................................. 27
Igor De Rycke and Jan Doutreloigne have used a top gate technology for realizing nTFT resp. CTFT circuits. This had certain advantages for optimizing the semiconductor properties. The technology of Doutreloigne is described.

The standard poly-CdSe active-matrix technology ....................................................... 30

This technology is described and it is explained that a bottom gate (plus a partial top gate) is essential because of the light sensitivity of CdSe.

Incompatibilities between the two technologies ........................................................... 31

It is shown that it is virtually impossible to join the existing CTFT and pixel technology on the same substrate.

2.2 Proposed new technology ............................................................................................ 32

The initially proposed unified technology is described. The number of lift-off steps is minimized to avoid problems with micro-hurs and the total number of mask steps is kept low.

2.3 Problems and solutions ................................................................................................... 33

Several technological problems have necessitated alterations of the new technology. There were problems with the Al gates. Using Cr created new problems. TiW proved to be a good alternative. The complicated combined semiconductor/source/drain etching step also caused problems, which were solved by re-introducing some non-critical lift-off steps. A curious problem was the fact that InAu no longer made good contact on Ge, which it did in the past. I was not able to explain this in a short term and for pragmatic reasons I had to find another source/drain-material for both CdSe and Ge. Ti works on Ge, but not on CdSe. TiW works on both, provided some thermal annealing steps are carried out.

2.4 The $V_T$-problem of Ge ............................................................................................... 36

Another mysterious problem is the fact that bottom gate Ge-TFT's have a totally different threshold voltage behaviour than their top gate equivalents. A lot of time was invested in tuning several process parameters in order to obtain the same characteristics as in the top gate technology. Unfortunately this did not lead to success. Some interesting conclusions can however be drawn from these experiments. There are also some ideas that could not be worked out, because of the time scheme that had to be followed.

2.5 The eventual technology .................................................................................................... 39

Just what the title says.

2.6 The eventual TFT-characteristics ...................................................................................... 41

MOSFET parameters that fit best with the resulting TFT characteristics.

Chapter 3 : Circuit design .......................................................................................................................... 43

3.1 Introduction .............................................................................................................. .............. 43

3.2 Literature study .......................................................................................................... ............. 43

Introduction : different classes of drivers ........................................................................ 43

Almost all driver circuits can be catalogued as commutators, scanners or SLB-drivers (Shift,Latch,Buffer). The difference between these is explained, as well as their typical (dis)advantages. We can also discriminate between two and multi grey level drivers, digital and analogue drivers, nMOS and CMOS drivers, ... Now follows a discussion of some interesting driver schemes that
have been published. [Note: it is almost impossible to summarize this discussion any further, because it is already very compact. Therefore I refer to the paper I have presented on the 1st CdSe workshop, which was in fact the base for this chapter.]

Morin et al., 1981

Oldest poly-Si driver circuit. Typical scanner. Uses memory capacitor for each column. Prone to image bending. As far as I know it was never realised.

Malmbarg et al., 1986

MiniGraphics displays. Typical commutator. Analogue driver, analogue grey levels. Driver can be used for fault location. Uses CdSe as semiconductor. Was realised and works.

Tizabi et al., 1986

First CTFT driver using CdSe (and Ge). Uses sample-and-hold modules in column driver. Disadvantage is hysteresis in buffer characteristics, which limits number of grey levels. Very low number of TFTs. Row driver probably not powerful enough to prevent image bending. I suspect the circuit was never realised.

De Rycke et al., 1988

SLB with CdSe. Clocks up to 2 MHz. Digital line memory. Needs parallelism for high resolution.

Ohwada et al., 1988

Commutator with 4 grey levels. TFTs only used as switches. Lots of crossovers in column driver. Powerful but complicated row drivers.

Matsueda et al., 1989

Hybrid scanner-commutator. 8-fold parallelism. Extremely redundant design (all pixels addressed via 2 totally independent ways). Driver circuit can be used for fault detection.

Emoto et al., 1989

Very sophisticated design. Uses parallelism without requiring pre-processing of video data. Analog RGB input. Surprisingly low number of TFTs per column.

R. Stewart et al., 1990

SLB driver with 32 grey levels. 100-fold parallelism. Uses chopped ramp type DAC’s. Complicated circuitry to be realised in thin-film technology.

Others

Some references to other interesting papers.

Summarizing table

This table systematically summarizes the most interesting features of the referenced driver circuits.

Solutions for the image bending problems with scanners

Leaving more time between consecutive lines is the classic way to do this. A more elegant approach would be to cut the gate lines in half and use two line scanners: the right one being delayed by half a line period compared to the left one. The only disadvantage is the fact that redundancy by two-sided addressing is no longer possible.

Methods for implementing grey levels

7 different methods for creating grey levels are discussed. One of them is original and uses ON/OFF subframes with different illumination intensity in order to avoid viewing angle dependence. Other methods use intermediate voltages, ON/OFF subframes with different select voltages, resulting in intermediate RMS voltages or (with fast responding LC materials) intermediate light impressions, N equivalent subframes resulting in N+1 possible grey levels, halftoning with extra TFT's or halftoning with capacitive voltage divider.
3.3 Discussion of chosen driver scheme .................................................................  60
   I have chosen a SLB-type circuit, comparable to the De Rycke type, but with
   complementary invertors or with depletion load invertors. Pass-TFT's are used
   instead of CMOS switches, because of the bad ON/OFF-ratio of the p-type
   TFT's. The operation of the driver is discussed in more detail. Especially the
   operation of the latch circuit (sense amplifier) requires some explanation.

3.4 Simulations ........................................................................................................  63

   Introduction..........................................................................................................  63
   After choosing a driver scheme, the components have to be dimensioned in
   order to optimize performance. A pure heuristic way, in which all possible
   combinations of gate width and length, etc. are actually realised and tried out,
   is far too expensive and too slow. Therefore, preliminary circuit simulations are
   necessary. Because of the large number of simulations that have been carried
   out, only some of the results are presented here.

Static invertor characteristics..................................................................................  64

   Terminology ......................................................................................................  64
   The notions 'stable operating points', 'astable operating point', 'noise
   margins' and 'gain' are introduced. Different invertor types are
   shown.

   Simulation results..............................................................................................  65
   It is shown that, given our depletion type Ge-TFT's, the depletion-load
   invertors yield the best static invertor characteristic.

Dynamic shift registers ...........................................................................................  67

   Terminology and criterion for proper operation..............................................  67
   A quantity $\Delta$ that describes the 'goodness' of the operation of a
   dynamic shift register is introduced. This allows us to use a limited
   number of simulations to predict the maximum operation frequency of
   the shift register.

   Simulation results..............................................................................................  68
   Dynamic shift registers with different invertor types and transistor
   geometries are simulated at different frequencies. The resulting $\Delta$'s of
   all these simulations are summarized in a number of graphs. This leads
   to an optimum value for the transistor geometries and it predicts a
   maximum clock frequency of 5 MHz for the depletion-load type shift
   register.

   Conclusion...........................................................................................................  71
   The depletion-load invertor behaves best in static both as dynamic circuits. A
   first indication of the ideal geometries can be given.

3.5 Other application: SSR for bargraph-display......................................................  72

   A possible application for thin-film circuits where speed is not the primary demand, is
   the addressing of multi-pixel guest-host LC displays, such as the bargraph-type
   displays. Passive multiplexing can not be used because of hysteresis in this type of LC
   material. Direct addressing becomes too expensive because of the high number of
   interconnections. Active addressing and an integrated static shift register can be
   fabricated with a high yield for such a low number of pixels and is therefore an
   attractive solution.

Chapter 4 : A better TFT-model for simulations.........................................................  75

   4.1 Introduction ..................................................................................................  75
   All simulations until now were performed using the SPICE Level 1 Schichmann &
   Hodges MOSFET model. In this chapter I propose a new, semi-heuristic, model that is
   an extension of this simple model, but with which the subthreshold behaviour and the
   superlinear 'linear' region can be described.
4.2 Static current equation

The Schichmann & Hodges current equations are written on one line, using the step function to account for the transitions between the different operating regions. A term representing the shunt resistance \( R_0 \) of a TFT is added. Then, a hyperbolic function with one parameter \( V_c \) (curvature voltage) is introduced to smooth the transitions between the regions. Finally, the squares in the current equation are replaced by the exponent \( \kappa \) in order to model the superlinear behaviour. The transconductance \( \beta \) is replaced by \( B \), the 'preterconductance', and \( \kappa \) is called the 'preterconductance exponent'. The resulting equation is a single-line formula describing the current in all operating regions (including sub-threshold) and requiring only 5 device parameters.

4.3 Dynamic behaviour

If we assume that the quasi-stationary approximation is valid, the dynamic effects can be described by introducing nonlinear terminal capacitances \( C_{GD} \) and \( C_{GS} \). These capacitances are also written as single-line formulas, requiring only three device parameters: \( V_c \), \( V_T \) and \( C_i \), the geometric gate insulator capacitance.

4.4 Implementation in simulation program

The new TFT model was implemented as a macro circuit with 6 parameters in a modern simulation program.

4.5 Parameter extraction and correspondence with measurements

Some algorithms are derived to extract the 6 model parameters from measurements of \( I_{DS}(V_{GS}) \) characteristics. It is illustrated that in this way, it is possible to achieve excellent agreement between model calculations and measurement over a large range of voltages.

4.6 Conclusion: pros and cons of the model

Advantages

- Simpler than Spice level 2 or 3; better than level 1; good subthreshold description, including shunt resistance; single-line formula, easy to implement in macro circuit; continuously derivable formulas, enhancing convergence speed of calculations; only 6 well-defined parameters, no parameter redundancy; easy parameter extraction from measurements; TFT modelled as a real 3-terminal device, no need to play tricks with the substrate potential.

Disadvantages

- Physical interpretation of \( V_c \) and \( \kappa \) is not immediately clear, temperature dependence is not taken into account; often not usable for MOSFET's, because there is no substrate terminal; the hyperbolic function was arbitrarily chosen for reasons of simplicity, probably another function could yield even better results; calculations are more complicated than with the SPICE level 1 model and require more CPU time.
platforms are changing rapidly, new solutions have to be found. I give an overview of the
different possibilities. The realisation of the masks was done by laser plotting (4000 dpi)
on a photographic foil and subsequent photolithographic copying onto TiW coated 5"x5" glass plates.

5.3 Detailed description of the mask sets..................................................................................... 92

In this section the mask sets are rather thoroughly described. This is especially useful for reference during future designs of new mask sets or adoptions of the present sets. I will only comment on those paragraphs that seem interesting enough for a `normal' reader of this manuscript.

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Design-rules and positioning ......................................................................................... 94
The modules ....................................................................................................................... 94

Includes a diagram of the hierarchy of the modules (also in the description of the following mask sets.)

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Many variants of the 'standard' technology are allowed.

Design-rules and positioning ......................................................................................... 99
The modules ....................................................................................................................... 99

Maskset 3 : MASK64 ................................................................................................... 103

Introduction ....................................................................................................................... 103

Pixel matrix. Safe design, but still a large aperture (54.25 % for a 20 by 20 units cell.) Unit is 25 µm.

Selection of masks........................................................................................................... 103
Order of process steps ...................................................................................................... 103
Design-rules and positioning ......................................................................................... 103
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Not only the unit cell, but also test-inserts.

Maskset 4 : DOGMA .................................................................................................... 106

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Personally I like Fig. 55 very much.

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DC-characteristics of simple invertors. ............................................................................. 118

Just what it says. Different inverter types are compared.

DC-characteristics of cascades of invertors............................................................................. 119

Ring oscillators ...................................................................................................................... 119

These were measured using a buffered probe with 12 pF input capacitance and later also using a picoprobe with 0.1 pF input capacitance and 1 MΩ input resistance. The delay time as a function of the geometric aspect ratio of the p-
channel TFT is evaluated for different invertor types. Also the turn-on voltage is studied, as explained in my contribution to the 3rd Intl. CdSe workshop.

6.4 Analogue switches......................................................................................................... 123
6.5 Static shift registers .................................................................................................... 124
   The operation at 6 kHz and at 400 kHz is shown. We did not have the picoprobe at the time of these measurements. A criterion for estimating the maximum number of pixels that can be addressed with the unbuffered static shift register, is derived.

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   Picture of an operating AMLCD with PN-LC from Dainippon Inc. My primary contribution to this demo is the addressing software.

6.9 Integrated drivers........................................................................................................ 133
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   The operation of the dynamic shift register in a complete driver circuit is illustrated.

Chapter 7: Conclusions ........................................................................................................................... 139
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   A new technology for making p-channel Ge TFTs with a staggered bottom gate structure, compatible with the poly-CdSe active matrix technology was constructed. Many technological problems had to be solved to achieve this. Published TFT-based driver circuit were intensively studied and compared. The relevant information was summarized in a systematic way. Different methods to produce grey scales were compared as far as image quality, viewing angle dependence, etc. are concerned and a new method was proposed. Based on all this information, a CTFT driver circuit was designed and network simulations were performed on the building blocks. An interesting application of a static shift register with TFTs was discussed. Stimulated by the difficulties in determining appropriate MOSFET model parameters from TFT measurements, a new, numerical, dedicated TFT model was constructed, requiring few parameters and representing the most important TFT features. This model is used in the present simulations and automatic parameter extraction is being implemented in our measurement software. A working driver circuit was realised in three steps, each with their own mask set. A new, safe 64×64 pixel active matrix design was the by-product. Electronics that were necessary to demonstrate the driver circuits were realized and used. I have designed a fault location system for our active matrices and I have written software for this interesting evaluation tool. I have also written software for the display demonstrator. The most important results of my research were reported in a number of publications.
What can still be done?........................................................................................................ 140

Many ideas for making enhancement type bottom gate Ge TFT's were not worked out. A demonstration of the 8×8 pixel matrices with integrated drivers could not take place because of yield problems.

7.2 The future .......................................................................................................................... 140

I present my personal opinion about how the results of this research project could be useful in industrial applications.

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I don’t believe this actually needs a summary.

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A pico-probe is only available since the beginning of 1993. For applying the 12 signal necessary for operation of a complete driver, elastomeric contacts were used.

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C.2 DC-characteristics of TFT’s .................................................................................................. 155

C.3 DC-invertor characteristics ................................................................................................... 156

C.4 Dynamic measurements ....................................................................................................... 156

An existing programmable digital signal generator with TTL outputs was provided with level shifters so voltages between 0 and 30 V could be achieved. The total circuit operates properly up to about 1.5 MHz. This and the 12 pF probe capacity has greatly limited the dynamic measurements.

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Herbert De Smet, November 10, 1993