FLYING CAPACITOR MULTILEVEL CONVERTER VOLTAGE BALANCE DYNAMICS FOR PURE RESISTIVE LOAD

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ABSTRACT

Multilevel converters need voltage balancing to be able to generate an output voltage with high quality. Flying capacitor converter topology has a natural voltage balancing property. Voltage balance dynamics analytical research methods reported to date are essentially based on a frequency domain analysis using double fourier transform. These complicated methods are not truly analytical, which makes an understanding of parameter influence on time constants difficult.

In this paper, a straightforward time domain approach based on stitching of switch intervals piece-wise analytical solutions to a DC modulated H-bridge flying capacitor converter is discussed. This method allows to obtain time-averaged discrete and continuous voltage balance dynamics models. Using small-parameter approximation for pure resistive loads, simple and accurate expressions for voltage balance time constants are deduced, revealing their dependence on load parameters, carrier frequency and duty ratio.

1. INTRODUCTION

Multilevel converters were developed as a result of a growing need for higher power converters, [1, 2]. In order to achieve this higher power rating, the voltage and current capabilities of the devices used in the converter need to be increased. Current insulated gate bipolar transistor (IGBT) technology extends up to 6.5 kV 900 A per switching device. Converters that make use of a series connection of switches, allow for the use of switches with reduced voltage ratings. These lower voltage switches have lower conduction losses and can switch at a higher frequency. Higher switching frequencies and a smaller voltage step capability result in higher quality switching waveforms.

Flying capacitor multilevel converters are an attractive choice

due to the natural voltage balance property. The balancing of the capacitors is driven by load current high order harmonics, [3, 4, 5, 6]. The capacitor voltage unbalance causes excessive energy dissipation in the converter load. Energy dissipation implies a resistive part in the load. So it can be intuitively seen that a load with a larger resistive part implies a faster balancing of the flying capacitors.

Flying capacitor converter voltage balance analysis methods are usually based on frequency domain transformations, [7]. The results of these analyses are not truly analytical and difficult to understand.

Reported flying capacitor converter analytical voltage balance research methods mostly deal with an AC modulation. By using the time domain analysis method, it's better to start from the DC modulation case. It can afterwards be extended to AC modulation.

This paper focuses on the balancing of flying capacitors in the case where the time constant of the load is smaller than the pulse width modulation (PWM) period, T_{pwm} . Starting from this condition, the calculation of the time constant can be done in a straightforward way, by using only time domain system models.

A straightforward time domain approach that is based on "stitching" of analytical transient solutions for consecutive PWM period switching subintervals to derive a DC modulated flying capacitor converter voltage balance dynamics model was applied in [8], assuming a inductance dominated load (load time constant T_L larger than T_{pwm}). Using a small-parameter technique, a single phase three level flying capacitor converter was first studied in [8]. Surprisingly simple accurate expressions for a voltage balance time constant revealing the dependence on load parameters, carrier frequency, and normalized voltage command (duty ratio) were obtained.

In this paper, the case of a resistance dominated load is stud-

ied. Voltage balance dynamics for the resistance dominated load, resulting high current ripple, is analyzed under the pure resistive load assumption. This gives a lower boundary of voltage balance time constants.

2. SINGLE PHASE 4-LEVEL CONVERTER TOPOLOGY AND MODULATION STRATEGY

A 4-level flying capacitor converter topology is depicted in Fig.1. Voltage modulation strategy for normalized voltage command $1/3 \leq D \leq 1$ is illustrated by Fig.2. The

Fig. 1. A 4-level flying capacitor multilevel converter circuit topology.

Fig. 2. Voltage modulation strategy for a 4-level flying capacitor converter for $1/3 < D < 1$.

instantaneous voltage command V_C is compared with triangular waves, one for each complementary switch pair. When the voltage command is higher then carrier wave c_i , S_i is switched on and $\bar{S}_i$ is switched off, for $i = 1, 2, 3$.

This PWM voltage modulation strategy creates a switch sequence that determines the output voltage. This output

voltage waveform is also depicted in Fig.2, assuming ideal switches and a balanced capacitors voltage, $V_{C1} = V_{DC}/3$ and $V_{C2} = 2V_{DC}/3$. For the moment, only $1/3 < D < 1$ is discussed. The case of $0 < D < 1/3$ will be handled further. A switching period is comprised of six intervals, as can be seen from Fig.2. In intervals 1, 2 and 3 (Fig. 3), at least one capacitor is connected to the power supply and the load. In interval 4, no capacitor is connected, so during this interval no balancing occurs.

The duration of an interval can be deduced from the PWM carriers, Fig. 2:

$$\begin{aligned} \Delta t_1 &= \Delta t_2 = \Delta t_3 = \frac{(1-D)}{2} T_{pwm}, \\ \Delta t_4 &= \frac{(D-1/3)}{2} T_{pwm}, \end{aligned} \quad (1)$$

with T_{pwm} the PWM period and $D = V_C / \frac{V_{DC}}{2}$, the normalized DC voltage command.

Fig. 3. Flying capacitor converter circuit topology for each switch interval for four level converter.

3. 4-LEVEL FLYING CAPACITOR CONVERTER DYNAMICS MODELING

3.1. Dynamics for $1/3 < D < 1$

For each switch interval, the flying capacitor converter can be modeled as a linear time invariant system. The 4-level single phase converter is a second order switched linear system with the capacitor voltages being the state variables. Therefore, for each switch interval state equations can be deduced for the capacitor voltage of both capacitors:

$$\begin{aligned} \mathbf{X}(t) &= \mathbf{A}_j(t) \mathbf{X}(0) + \mathbf{B}_j(t) \frac{V_{DC}}{2}; \\ \mathbf{X}(t) &= [V_{C1}(t) \quad V_{C2}(t)]^T; j = 1, \dots, 8. \end{aligned} \quad (2)$$

The state space matrix A and vector B are obtained by solving linear time invariant differential equations on individual

switching intervals. The topology in interval 1 (Fig. 3(a)) leads to following matrices:

$$A_1 = \begin{bmatrix} \exp(-t/T_1) & 0 \\ 0 & 1 \end{bmatrix}, \quad (3)$$

$$B_1 = \begin{bmatrix} 1 - \exp(-t/T_1) \\ 0 \end{bmatrix}, \quad (4)$$

with $T_1 = RC_1$.

For interval 2 (Fig. 3(c)), with both capacitors connected:

$$A_2 = \begin{bmatrix} \frac{C_2 \exp(-\frac{t}{T_2}) + C_1}{C_1 + C_2} & \frac{-C_2 \exp(-\frac{t}{T_2}) + C_2}{C_1 + C_2} \\ \frac{-C_1 \exp(-\frac{t}{T_2}) + C_1}{C_1 + C_2} & \frac{-C_1 \exp(-\frac{t}{T_2}) + C_2}{C_1 + C_2} \end{bmatrix}, \quad (5)$$

$$B_2 = \begin{bmatrix} \frac{C_2 \left(1 - \exp(-\frac{t}{T_2})\right)}{C_1 + C_2} \\ \frac{C_1 \left(1 - \exp(-\frac{t}{T_2})\right)}{C_1 + C_2} \end{bmatrix}, \quad (6)$$

with $T_2 = \frac{C_1 C_2}{C_1 + C_2} R$.

And for interval 3 (Fig. 3(b)):

$$A_3 = \begin{bmatrix} 1 & 0 \\ 0 & \exp(-t/T_3) \end{bmatrix}, \quad (7)$$

$$B_3 = \begin{bmatrix} 0 \\ 1 - \exp(-t/T_3) \end{bmatrix}, \quad (8)$$

with $T_3 = RC_2$.

By combining the equations for each interval, a discrete model is obtained "averaged" over a PWM period:

$$\begin{aligned} X(T_{pwm}) &= AX(0) + B \frac{V_{DC}}{2}, \\ A &= A_3 A_2 A_1, \\ B &= A_3 (A_2 B_1 + B_2) + B_3. \end{aligned} \quad (9)$$

These matrices A and B depend on D, because the interval duration depends on D and these expressions are filled in the matrices A_j and B_j for each switch interval.

The real eigenvalues of matrix A can be used to deduce the continuous averaged system time constants. This methods gives a complicated expression. By using a further approximation, a shorter expression can be deduced. For pure resistive load, it is possible to do an approximation under a small-parameter assumption given by the inequality:

$$T_{pwm} \ll \min(T_1, T_2, T_3), \quad (10)$$

with T_1 and T_2 the time constants of voltage over capacitors 1 and 2. This means there is no significant capacitor voltage

change on a single PWM period. This small-parameter assumption does not include the load time constant, because the absence of inductance.

Suppose $V_{DC} = 0$ and pre charged capacitors at their normal voltage. This results in free capacitor discharge (homogenous system). Assumption (10) leads to following equations for interval 1:

$$\Delta V_1 = \frac{V_1(0) \Delta t}{RC_1}; \Delta V_2 = 0, \quad (11)$$

for interval 2:

$$\Delta V_2 = \frac{V_2(0) \Delta t}{RC_2}; \Delta V_1 = 0, \quad (12)$$

and for interval 3:

$$\begin{aligned} \Delta V_1 &= \frac{(V_1(0) - V_2(0)) \Delta t}{RC_1}; \\ \Delta V_2 &= \frac{(V_2(0) - V_1(0)) \Delta t}{RC_2}. \end{aligned} \quad (13)$$

Δt is for every interval $\frac{(1-D)}{2} T_{pwm}$. Combining (11)-(13) leads to:

$$\begin{aligned} \Delta V_1 &= \frac{(2V_1(0) - V_2(0)) (1-D) T_{pwm}}{2RC_1}; \\ \Delta V_2 &= \frac{(2V_2(0) - V_1(0)) (1-D) T_{pwm}}{2RC_2}. \end{aligned} \quad (14)$$

Using average derivatives approximations

$$\frac{dV_1}{dt} \approx \frac{\Delta V_1}{T_{pwm}}; \frac{dV_2}{dt} \approx \frac{\Delta V_2}{T_{pwm}}, \quad (15)$$

the discrete equation (14) can be approximated by a differential equation:

$$\begin{bmatrix} \dot{V}_1 \\ \dot{V}_2 \end{bmatrix} = \frac{1-D}{2R} \begin{bmatrix} 2/C_1 & -1/C_1 \\ -1/C_2 & 2/C_2 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}. \quad (16)$$

Combining a solution of the homogeneous equation (16) with a forced solution for non-zero voltage supply - balanced capacitor voltages equal to $V_{DC}/3$ and $2V_{DC}/3$ respectively, a general solution can be obtained. This general solution is too bulky to depict here.

For equal capacitances $C_1 = C_2 = C$, an averaged voltage balance dynamics solution for non zero supply voltage is given by following equations:

$$\begin{aligned} V_1(t) &= \frac{V_{DC}}{3} + \left(\frac{V_1(0) + V_2(0) - V_{DC}}{2} \right) \exp\left(\frac{-t}{T_C}\right) \\ &\quad - \left(\frac{V_2(0) - V_1(0) - V_{DC}/3}{2} \right) \exp\left(\frac{-t}{T_D}\right); \end{aligned} \quad (17)$$

$$\begin{aligned} V_2(t) &= \frac{2V_{DC}}{3} + \left(\frac{V_1(0) + V_2(0) - V_{DC}}{2} \right) \exp\left(\frac{-t}{T_C}\right) \\ &\quad - \left(\frac{V_2(0) - V_1(0) - V_{DC}/3}{2} \right) \exp\left(\frac{-t}{T_D}\right), \end{aligned} \quad (18)$$

with differential and common mode time constants:

$$\begin{aligned} T_D &= \frac{2RC}{3(1-D)}, \\ T_C &= \frac{2RC}{1-D}. \end{aligned} \quad (19)$$

3.2. Dynamics for $0 < D < 1/3$

The voltage modulation strategy for $0 < D < 1/3$ is depicted in Fig. 4. The interval durations can be deduced from Fig. 4:

Fig. 4. Voltage modulation strategy for 4-level flying capacitor converter for $0 < D < 1/3$.

$$\begin{aligned} \Delta t_1 &= \Delta t_2 = \Delta t_3 = \frac{(1/3 + D)}{2} T_{pwm}; \\ \Delta t_5 &= \Delta t_6 = \Delta t_7 = \frac{(1/3 - D)}{2} T_{pwm}. \end{aligned} \quad (20)$$

Although conduction paths differ, the instantaneous equivalent circuit topology for switch intervals 5, 6 and 7 are the same as in 3, 1 and 2, respectively. This means the effect on the capacitor voltage is the same in the corresponding switch intervals.

Combining the switch interval durations for the same capacitor voltage effect results in:

$$\Delta t_1 + \Delta t_6 = \Delta t_2 + \Delta t_7 = \Delta t_3 + \Delta t_5 = \frac{T_{pwm}}{3}. \quad (21)$$

This proves that for $0 < D < 1/3$ voltage balance dynamics do not depend on D and are identical to that for $D = 1/3$.

4. H-BRIDGE 3-LEVEL CONVERTER TOPOLOGY AND MODULATION STRATEGY

H-bridge 3-level flying capacitor converter topology is depicted in Fig. 5. H-bridge converter double carrier phase shifted voltage modulation is demonstrated in Fig. 6. Carrier c_{13} delivers switch states for switch pair 1 (with V_C) and switch pair 3 (with $-V_C$). As can be seen from Fig. 6, a switching (PWM) period is comprised of eight intervals for normalized voltage command D .

Fig. 5. A 3-level H-bridge flying capacitor multilevel converter circuit topology.

Fig. 6. Voltage modulation strategy for a 3-level H-bridge flying capacitor converter topology for $0 < D < 1/2$.

4.1. Dynamics modeling for $0 < D < 0.5$

Corresponding topologies for each switch interval generating load voltage $V_{DC}/2$ are depicted in Fig. 7; topologies for each switch interval generating zero load voltage, $V_L = 0$ are depicted in Fig. 8.

Duration of the switch intervals can be deduced from carriers in Fig. 6:

$$\begin{aligned} \Delta t_1 &= \Delta t_3 = \Delta t_5 = \Delta t_7 = \frac{D}{2} T_{pwm} \\ \Delta t_2 &= \Delta t_4 = \Delta t_6 = \Delta t_8 = \frac{0.5 - D}{2} T_{pwm} \end{aligned} \quad (22)$$

Just like in the 4-level case, for every switch interval a linear time invariant system can be deduced with state equations (2). As the instantaneous topologies are similar to those of the 4-level case, the same matrices A_j and B_j for corresponding switch intervals can be chosen. For switch intervals 1 and 5, there is no voltage supply in the topology, so B_j is a zero vector in this case.

A similar homogeneous system as for the 4-level converter can be calculated and with assumption (10) a similar approximation can be made. This results in similar equations as (11)-

Fig. 7. Flying capacitor converter circuit topology for each switch interval for 3-level H-bridge converter (1).

Fig. 8. Flying capacitor converter circuit topology for each switch interval for 3-level H-bridge converter (2).

(13) for each switch interval.

Combining these equations and filling in the time interval results in:

$$\begin{aligned} \Delta V_1 &= \frac{V_1 - (1 - 2D)V_2}{2RC_1}; \\ \Delta V_2 &= \frac{V_2 - (1 - 2D)V_1}{2RC_2}. \end{aligned} \quad (23)$$

Resulting in approximated differential equations:

$$\begin{bmatrix} \dot{V}_1 \\ \dot{V}_2 \end{bmatrix} = \frac{1}{2R} \begin{bmatrix} 1/C_1 & -\frac{1-2D}{C_1} \\ -\frac{1-2D}{C_2} & 1/C_2 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}. \quad (24)$$

For equal capacitances $C_1 = C_2 = C$, an averaged voltage balance dynamics solution for non zero supply voltage is given by following equations:

$$V_1(t) = \frac{V_{DC}}{2} + \left(\frac{V_1(0) + V_2(0) - V_{DC}}{2} \right) \exp\left(\frac{-t}{T_C}\right) - \left(\frac{V_2(0) - V_1(0)}{2} \right) \exp\left(\frac{-t}{T_D}\right); \quad (25)$$

$$V_2(t) = \frac{V_{DC}}{2} + \left(\frac{V_1(0) + V_2(0) - V_{DC}}{2} \right) \exp\left(\frac{-t}{T_C}\right) - \left(\frac{V_2(0) - V_1(0)}{2} \right) \exp\left(\frac{-t}{T_D}\right), \quad (26)$$

with differential and common mode time constants:

$$\begin{aligned} T_D &= \frac{RC}{1-D}, \\ T_C &= \frac{RC}{D}. \end{aligned} \quad (27)$$

4.2. Dynamics modeling for $0.5 < D < 1$

For $0.5 < D < 1$ topologies 2, 4, 6 and 8 are replaced by topology 9, Fig. 8(d). Because the balancing of the capacitors is now totally independent, the dynamic modeling becomes almost trivial.

$$T_1 = \frac{RC_1}{1-D}; T_2 = \frac{RC_2}{1-D} \quad (28)$$

5. SIMULATIONS

Simulations were carried out with $T_{pwm} = 0.001s$, $R = 3\Omega$, $C_1 = C_2 = 200\mu F$, $V_{dc} = 100V$.

5.1. 4-level single phase simulations

A first simulation is depicted in Fig. 9 with both capacitors uncharged. The instantaneous capacitor voltages are compared with the results of equations (17) and (18).

Fig. 9. Simulated capacitor balancing of 4-level converter with D=0.75.

5.2. 3-level H-bridge simulations

The simulations of capacitor balancing for the 3-level H-bridge converter topology are depicted in Fig. 10 (both capacitors uncharged, common mode) and Fig. 11 ($V_{C_1} = 100V$ and $V_{C_2} = 0V$, differential mode).

Fig. 10. Simulated capacitor balancing of 3-level H-bridge converter with $D=0.25$.

Fig. 11. Simulated capacitor balancing of 3-level H-bridge converter with $D=0.25$.

6. CONCLUSIONS

A time domain approach to construct a family of flying capacitor converter dynamics models by stitching of analytical solutions for consecutive switching intervals is presented.

For DC modulation the model is linear time-invariant, which makes the dynamics analysis straightforward.

For 4-level single phase and 3-level H-bridge converter topologies, we obtained simple and accurate expressions for voltage balance time constants and capacitor voltage balance dynamics for the case of a resistive load by applying the small-parameter technique. The expressions for differential and common mode voltage balance time constants reveal the voltage balance rate's dependence on carrier frequency, capacitance of flying capacitors and the load.

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