Ultra-compact, low power consumption silicon photonic/electronic QPSK/16-QAM coherent receiver operating at 28GBaud

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Abstract: We demonstrate the co-integration of an ultra-compact silicon photonic receiver and a low power consumption (155mW/channel) 2-channel linear transimpedance amplifier array. Operation below FEC threshold both for QPSK and 16-QAM at 28 Gbaud is demonstrated.

Index Terms: Coherent receivers, Silicon photonics, Electronic-photonic co-integration.

1. Introduction

The growth of internet traffic of over 60% per year requires a constant evolution in transceiver technology in order to cope with the increasing demand. This has resulted in the deployment of 100Gbit/s Ethernet coherent transceivers in long-haul networks, while a large effort is already dedicated to the evolution towards 400Gbit/s. The major advantages of coherent communication include its spectral efficiency as well as the electronic compensation of linear and non-linear impairments of the transmission link [1]. In the near future coherent transceivers are expected to become key components in metropolitan area networks and on the longer term they most likely will also penetrate the access domain [2,3,4]. While coherent transceivers are already being used for backbone and metro networks, the size, power dissipation and cost of these transceivers need to be significantly reduced for use in access networks. Photonic integration is considered as the only viable route to realize such compact, low-cost and low-power transceivers. Several photonic integration platforms are being considered for the implementation of these devices including the use of planar lightwave circuits [5], InP-based photonic integrated circuits [6] and silicon photonics [7]. For applications in access, silicon photonic coherent transceivers have a great potential. The high refractive index contrast available on this platform allows for ultra-compact devices. In addition, to allowing ultra-compact devices, the high refractive index contrast of this platform also allows for the straightforward integration of polarization diversity, either by using two-dimensional grating structures [8] or polarization-insensitive spotsize converters combined with a polarization rotator [9]. The compact size of silicon photonic integrated circuits, together with the economies of scale of silicon processing enable at the same time low-cost chips. No hermetic packaging of these devices is required, thereby further reducing the cost and size of the overall packaged device. While in a classical integrated photonics coherent transceiver the photonic device footprint is mainly determined by long phase modulators [10], for access networks we envisage the implementation of the IQ modulator using electro-absorption modulators (EAMs) [11,12], as shown

in Figure 1. Such modulators are much more compact (50 to 100 µm device length) compared to the classical traveling wave phase modulators. Recently, first generation III-V-on-silicon EAMs [13] and Ge EAMs [14] integrated on the silicon photonic platform have been reported, operating at 28Gbit/s and 56Gbit/s respectively.

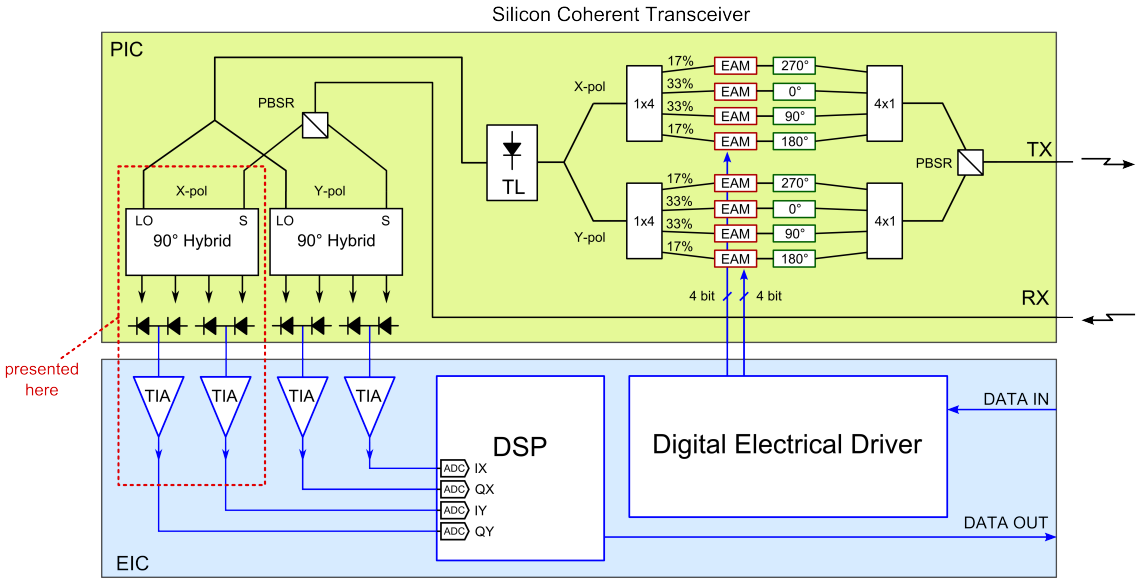

Figure 1: Envisaged silicon photonic coherent transceiver consisting of an electronic (EIC) and photonic (PIC) integrated circuit. In this paper the ultra-compact coherent receiver with integrated low-power consumption linear TIA array is demonstrated.

The power consumption of the coherent transceiver for access is mainly determined by the modulator drivers and transimpedance amplifiers. Digital signal processing also contributes, but as the transmission distance in access networks is small, the required computational complexity is limited. Also, with the advancement of CMOS technology, the cost and power consumption of digital computations constantly decreases over time. On the transmitter side very low power consumption Ge EAMs (12fJ/bit dynamic power consumption) have been demonstrated [14]. Besides reducing the device footprint (and hence the cost) as discussed above, a transmitter based on EAMs therefore also reduces the power consumption of the transceiver considerably.

This paper reports on the realization of an important sub-block of the silicon coherent transceiver as indicated in Figure 1: an ultra-compact coherent receiver (0.3 mm by 0.7 mm) co-integrated with a low power consumption linear transimpedance amplifier array. The photonic IC is realized using imec's iSIPP25G platform. The device is based on a multi-mode interference 90° optical hybrid that has a very small footprint (13.7 µm by 155 µm) and does not require any DC control for adjusting the relative phases between the output ports. This reduces power consumption and decreases chip size. The 90° hybrid is connected to a pair of balanced high speed Ge photodetectors. By implementing the photocurrent subtraction on the photonic chip the number of bond pads required is reduced, leading to a further decrease in the photonic IC size. Also, because no decoupling capacitors are required on the photonic chip, the chip size can be further reduced. While in this proof-of-principle demonstration a single polarization receiver is described, a polarization-multiplexed coherent receiver with optimally placed grating coupler structures would only occupy about 0.5 mm by 0.5 mm. The 2-channel linear single-ended input transimpedance amplifier (TIA) array is designed in 0.13-µm SiGe BiCMOS technology. Besides for linearity, the electronic circuit is optimized for low power consumption. As will be discussed later, a single TIA operating at 28Gbaud consumes only 155 mW, a substantial improvement over previous demonstrations [15,16]. In this work, 28 Gbaud quadrature phase shift keying (QPSK) and 16-quadrature amplitude modulation (16-QAM) reception is demonstrated using the silicon coherent receiver integrated with the 2-channel TIA array. In both cases the receiver can operate below the forward error coding (FEC) limit (3.8×10^{-3} at 7% overhead). For QPSK less than 12 dB/0.1 nm

optical signal to noise ratio (OSNR) is required to realize this, 2.5 dB above the theoretical limit.

This paper is organized as follows: in Section 2, the design and characterization of the silicon photonic integrated circuit is described. In Section 3, the design of the low-power linear TIA array is discussed, while in Section 4 the co-integration and the system experiments are described.

2. Silicon photonic integrated circuit design and characterization

The silicon photonic integrated coherent receiver is realized in imec's iSIPP25G platform. The layout of the circuit is shown in Figure 2(a). The circuit occupies an area of 0.3 mm by 0.7 mm. It consists of single polarization fiber-to-chip grating couplers for coupling the advanced modulation format signal and local oscillator to the chip. By properly positioning the grating couplers, the size of the coherent receiver can be further reduced to be less than 0.45mm by 0.25mm.The fiber-to-chip grating coupler efficiency is -6.5 dB at a wavelength of 1550 nm. The -1dB bandwidth is 20 nm. Higher efficiency single polarization grating couplers [17] as well as two-dimensional grating couplers for polarization diversity [8] can also be realized on this platform. Implementing polarization diversity using a focusing two-dimensional grating coupler would increase the device footprint only to about 0.5 mm by 0.5 mm. The 90° hybrid is realized using a 2x4 multi-mode interference coupler. Compared to the recently reported silicon photonics single polarization coherent receiver [18] the use of a multi-mode interference coupler leads to a smaller footprint and does not require additional thermal tuners to control the relative phases at the output of the 90° hybrid. As discussed above, this in turn reduces the number of bond pads, which further reduces the chip-size and cost. The layout of the 2X4 multimode interference coupler is shown in Figure 2(b). The back-end dielectric stack is removed for clarity. The device consists of deeply etched entrance and exit waveguides defined in a 220 nm thick waveguide layer, while the MMI itself is shallow etched (70 nm) in order to reduce phase errors and power imbalance at the output. The nominal device parameters are MMI_L=115.5 µm, MMI_W=7.7 µm, Port_W=1.5 µm, Port_gap= 0.07 µm, TR_W=3 µm. The simulated wavelength dependence of the phase difference between the different output ports is shown in Figure 2(c). Here $\varphi_{ijk}= \varphi_{ij} - \varphi_{ik}$. φ_{ij} is the phase delay from input In_i to output ch_j, $\Delta\varphi_1=(\varphi_{11}- \varphi_{21})-(\varphi_{14}- \varphi_{24})-\pi$ and $\Delta\varphi_2=(\varphi_{12}- \varphi_{22})-(\varphi_{13}- \varphi_{23})- \pi$. Assuming an allowable phase difference deviation of +/- 5°, operation over the C-band is achieved. The simulated common mode rejection ratio ($CMMR = 20*\log10((T_{ij}-T_{ik})/(T_{ij}+T_{ik}))$, with T_{ij} the power transmission from input In_i to output ch_j, is better than -25 dB over the C-band

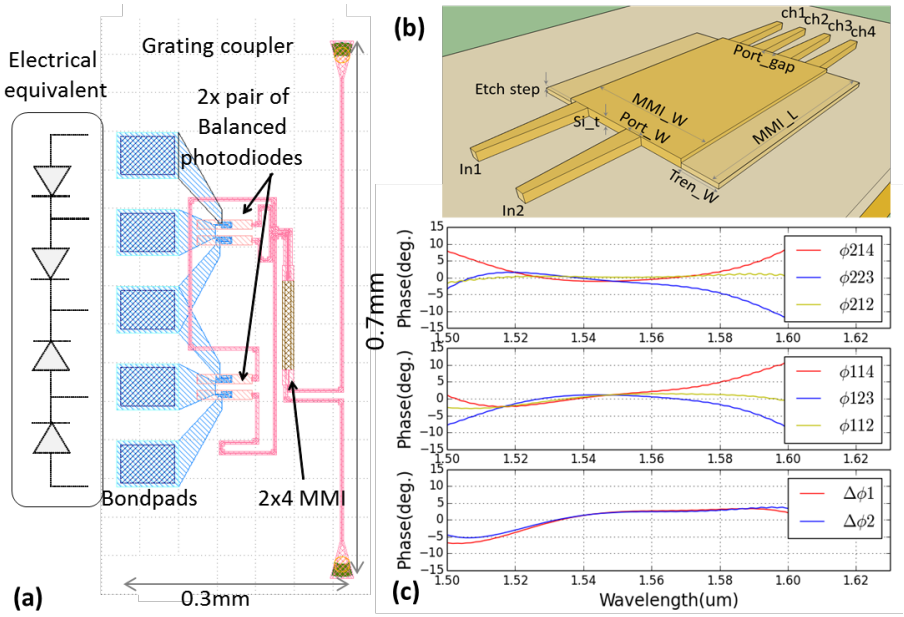

Figure 2: (a) layout of the single polarization coherent receiver with a footprint of 0.3 mm by 0.7 mm. (b) layout of the 90° hybrid defined on imec's iSIPP25G platform. (c) Simulation of the wavelength dependence of the 90° hybrid.

The fabrication tolerance of the MMI was assessed. Figure 3 shows the phase relations as a function of MMI length, width, etch depth and Si waveguide layer thickness, at a wavelength of 1550 nm (the wavelength used in the experimental work). For typical tolerances in fabrication (+/- 10 nm in waveguide widths and lengths, +/- 10 nm on etch depth and +/- 5 m on silicon waveguide layer thickness, phase errors below 5° are obtained. Simulations (not shown here) also indicate that the CMRR remains better than -20 dB in this fabrication window.

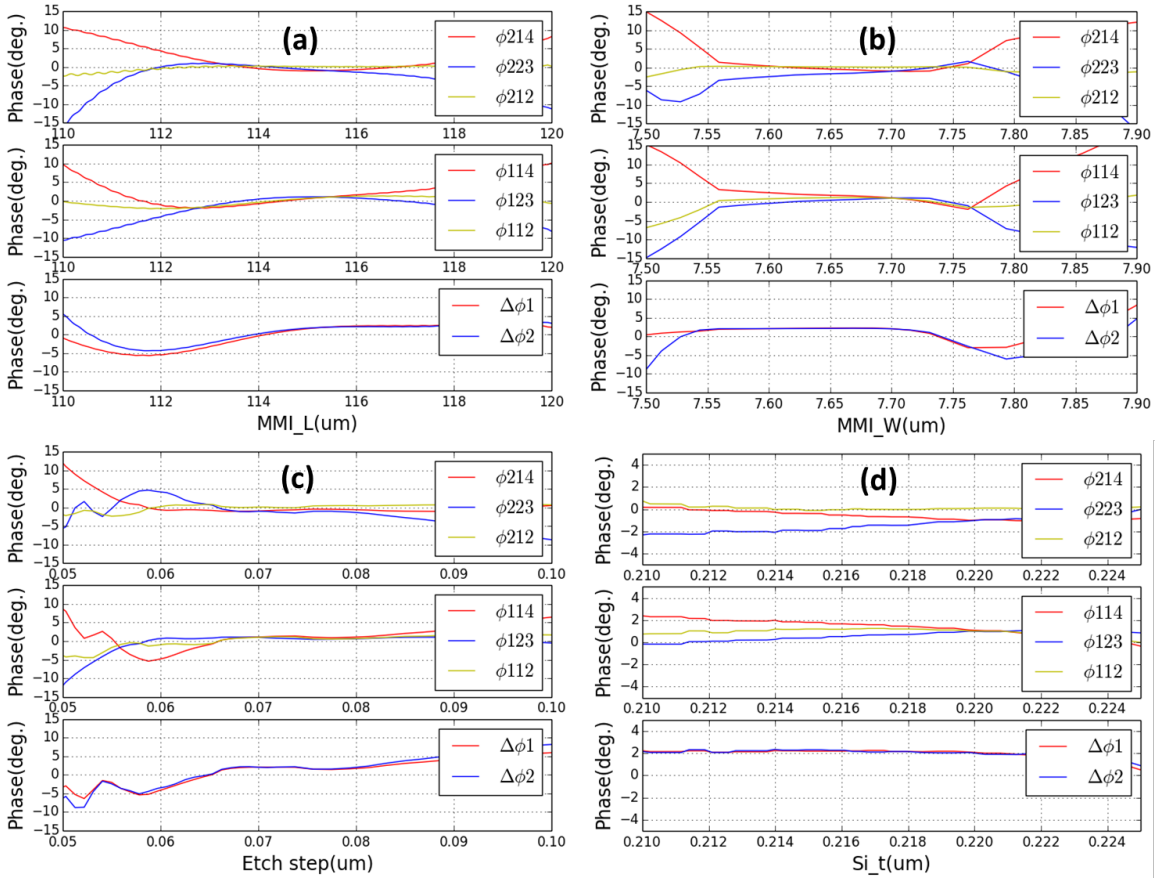

Figure 3: Tolerance analysis on the phase relations of the ultra-compact 90° hybrid used in this work. (a) influence of the length of the MMI coupler; (b) influence of the MMI width; (c) influence of the MMI etch depth; (d) influence of the silicon waveguide thickness.

High-speed germanium photodetectors are implemented at the output of the 90° hybrid. The characteristics of an individual photodiode integrated on the same chip as the coherent receiver are shown in Fig. 4. The individual photodetectors have a bandwidth above 50 GHz at – 1 V bias due to the low junction capacitance, a dark current of a <15 nA at – 1 V bias and an on-chip responsivity of 0.5 A/W. Good uniformity over 200 mm wafers is obtained [19], important for chip yield and hence cost reduction. On-chip subtraction of the photocurrent was implemented in order to reduce the number of bondpads required (and thereby again the chip-size). While this approach doubles the capacitance of the optical receiver and thereby reduces the bandwidth [20], the high bandwidth of the individual photodetectors still allows for 28 Gbaud operation as will be demonstrated below. Also, the on-chip current subtraction prevents a substantial DC photocurrent from the photodiodes to be injected in the transimpedance amplifier, simplifying the design.

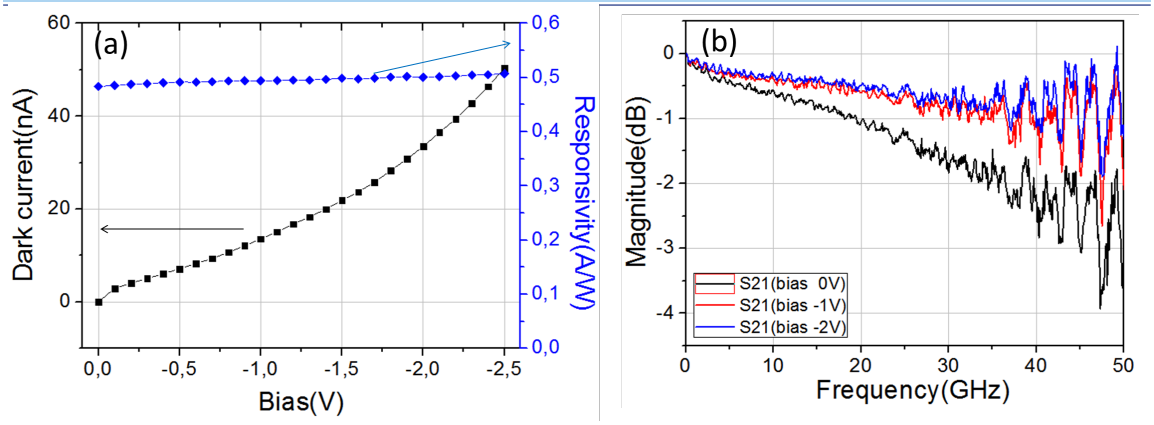

Figure 4: Ge PD characterization (single element photodiode implemented close to the integrated receiver): (a) IV characteristic and responsivity as a function of reverse bias; (b) Normalized S21-parameter of the photodetector used in the coherent receiver as a function of reverse bias.

3. SiGe BiCMOS linear trans-impedance amplifier array design

The transimpedance amplifier array, presented in [21,22], is fabricated in a 0.13-µm SiGe BiCMOS technology and consists of 2 identical TIAs in a mirrored configuration sharing a common ground, 2.5 V supply and bias voltage for the balanced photodiodes (set at ~2.2 V in the experiments). Furthermore, the serial peripheral interface controller is shared and a single bias block provides a 100 µA reference current to each TIA. The total chip area is 3000 µm x 900 µm of which each TIA occupies 1100 µm x 900 µm. A micrograph of the TIA array with annotated functional blocks and sizing is provided in Fig. 5.

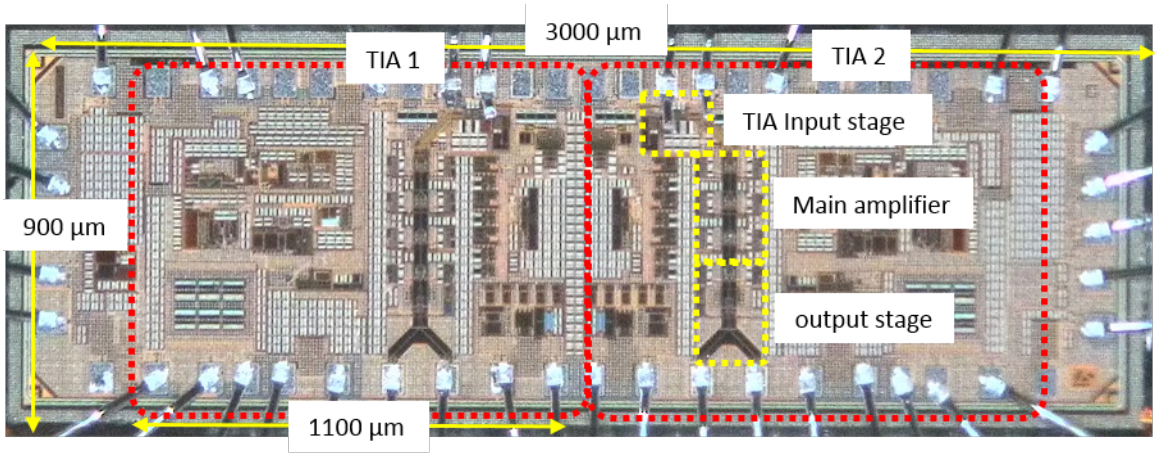

Figure 5: top-view of the two-channel TIA with an indication of the position of the different functional blocks.

Fig. 6 shows a simplified block diagram of the electrical equivalent of the coherent receiver and the TIA-array. The electrical signal path consists of a transimpedance input stage, a main amplifier and an output stage. The input stage converts the differential photocurrent I_{pd1}-I_{pd2} to a voltage signal through the feedback resistor R_F, which is implemented as an array of 8 parallel nMOS transistors operated in their linear region. As such, the transimpedance gain of this stage can be controlled digitally by turning on (decreasing R_F) or off (increasing R_F) transistors from this array. As the gain is typically inversely proportional to the bandwidth, a trade-off needs to be made in choosing the transimpedance. Figure 7(a) shows the simulated 3dB bandwidth of the TIA as a function of the transimpedance. Figure 7(b) shows the simulated transimpedance gain of the TIA as a function of frequency for R_F=133Ω, as used in the experiment.

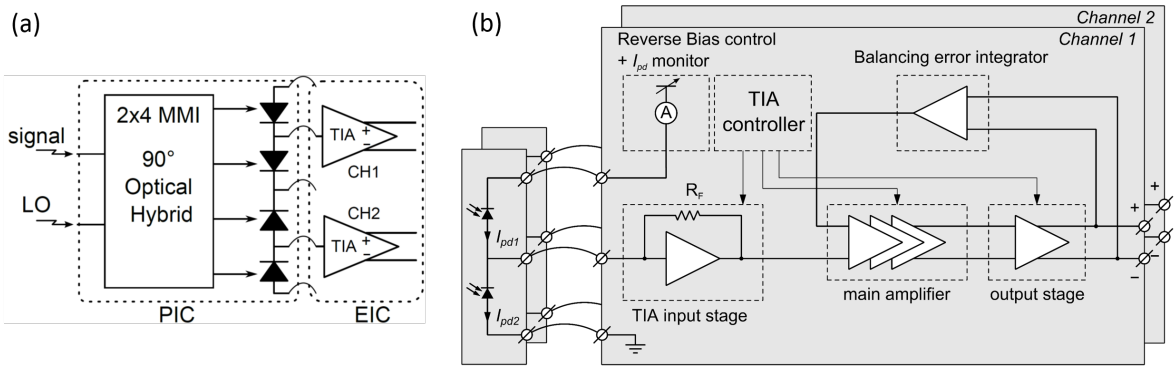

Figure 6: (a) block diagram of the integration of the silicon PIC with the 2-channel TIA array. (b) TIA architecture + biasing scheme of photodiodes;

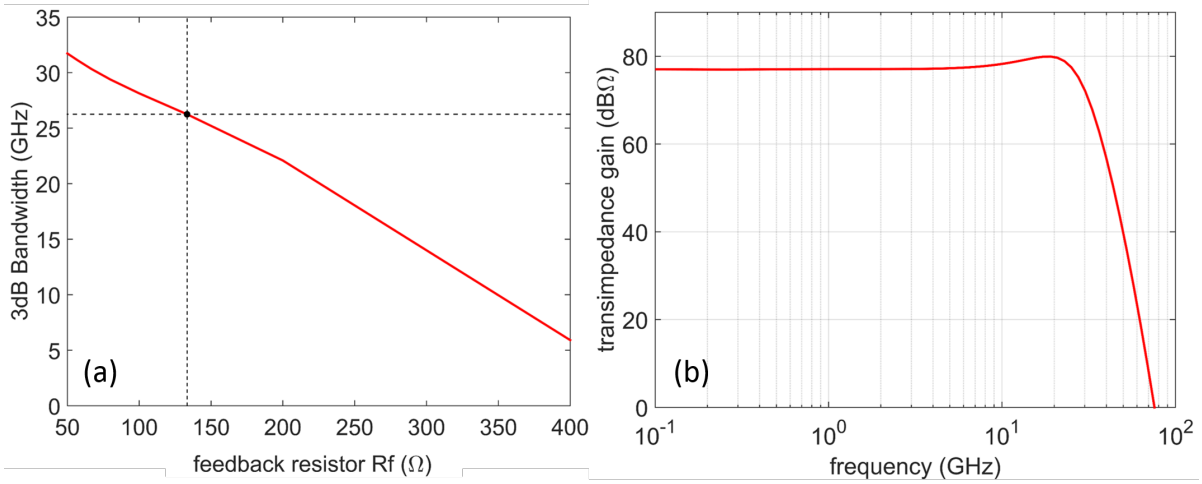

Figure 7: (a) simulation of the TIA bandwidth as a function of the transimpedance (b) simulated transimpedance gain of the TIA as a function of frequency for R_F=133Ω, as used in the experiment

4. Electronic/photonic co-integration and system experiments

While recently the monolithic integration of a coherent receiver and trans-impedance amplifier has been proposed and demonstrated [16], A hybrid integration is preferred over a monolithic approach in this work as it allows independent optimization of the used technology for the photonics and electronics, reducing the cost and allowing for commercial silicon foundry services to be used. The developed silicon photonic coherent receiver and transimpedance amplifier array were integrated on a 4-layer printed circuit board (PCB). Figure 8(a) shows the PCB used for testing purposes. The PCB was not minimized in size as to enable easy testing and assembly. Both dies were placed in a cavity in the center of the PCB as to minimize the required wire bond length between the transimpedance amplifier and the traces on the PCB. Care was taken during the assembly to place the 2-channel TIA-die (3 mm x 0.9 mm) and the silicon PIC as close as possible together in order to also minimize the lengths of the interconnection wire bonds. The 2x2 differential outputs of the two-channel TIA were routed symmetrically to 4 high-speed connectors at the edge of the board. Due to limitations of the measurement setup in the lab all measurements were however done single ended by terminating the corresponding output of the differential signal with a DC-block and a 50 Ω termination. Figure 8(b) shows a close-up of the wire bonded electronic and photonic die on the PCB.

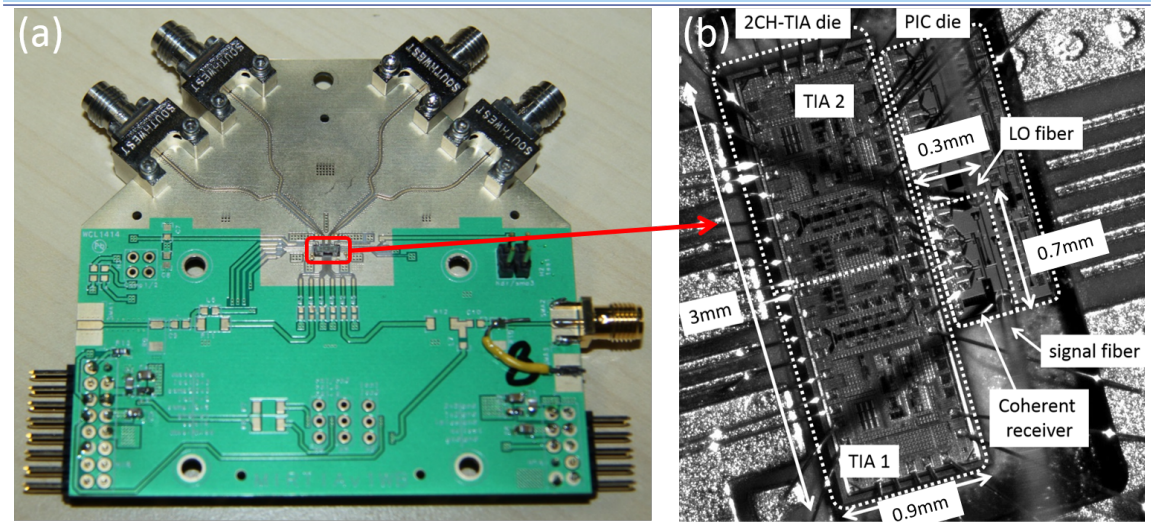

Figure 8: (a) View of the PCB used for testing purposes with the integrated silicon photonic coherent receiver and trans-impedance amplifier array (b) Close-up of the wire bonded electronic and photonic die on the PCB.

The measurement setup to characterize the coherent receiver at 28 Gbaud is shown in Figure 9. At the transmitter side the light of a C-band external cavity laser operating at 1550.92 nm (linewidth 100 kHz) is split, to be used both as local oscillator (LO) and signal. The signal part is guided through a $LiNbO_3$ Mach-Zehnder IQ-modulator (IQ-MZM) where it is modulated with a 2^{15}-1 long pseudo random bit sequence (PRBS) signal at 28 Gbaud and amplified by an EDFA. The IQ-MZM is driven by 2 digital-to-analog converters (DACs) to generate the in-phase and quadrature parts of the symbols. Both QPSK (2 bits/symbol) and 16-QAM (4 bits/symbol) modulation formats are generated for this study. For OSNR measurements, amplified spontaneous emission (ASE) noise is added to the modulated signal in a noise loading stage, where a variable optical attenuator provides the desired signal power to the receiver. At the receiver side, the amplified local oscillator is connected to the coherent receiver where polarization controllers allow efficient coupling of TE polarized light into the silicon photonic receiver through the fiber-to-chip grating couplers. The output of the TIA is read out by a 50 GHz 160 GS/s real-time oscilloscope. In the digital domain, the captured data is parallel processed offline in a distributed digital signal processing cloud. First, the digitized signals are down-sampled to 56 GS/s (for 2-fold oversampling), before optical front-end impairments are compensated. Then the data is processed by a minimum mean squared error (MMSE) time domain equalizer (TDE). The weight coefficients of the TDE are heuristically updated, with a variable step size [23], using the least mean squares (LMS) algorithm for convergence, and decision directed LMS for transmission. Note that TDE is employed instead of frequency domain equalizers due to their lower adaptation gain, which is too slow for stabile convergence while still maintaining enough symbols for accurate BER analysis. For the weight matrix, every capture contains 560k symbols, of which the least means squares (LMS) update algorithm for convergence switches after 40k symbols to decision directed least means squares (DD-LMS). Note that both algorithms have variable step-sizes [24]. Subsequently, the small frequency offset between the transmitter and local oscillator lasers is removed by applying carrier phase estimation based on digital phase locked loops [23]. Next, the symbols are demapped and the system BER is averaged over 1 and 2 million bits, for QPSK and 16QAM respectively.

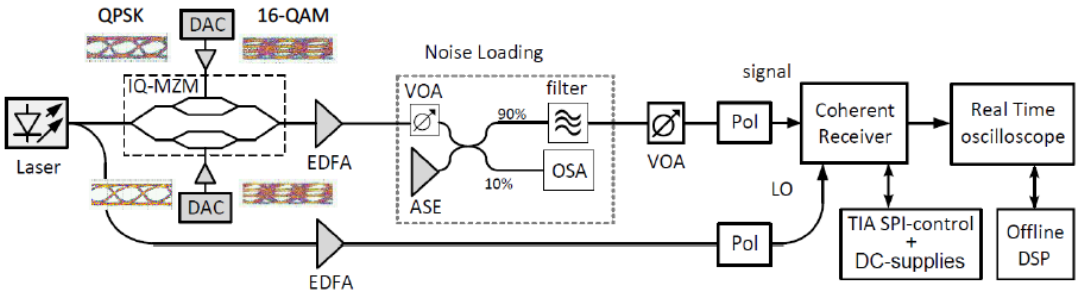

Figure 9: Schematic of the characterization setup of the receiver for QPSK and 16-QAM modulation

No temperature control of the photonic integrated circuit is used during the measurements. For the 28 Gbaud QPSK measurement 12 dBm fiber-coupled LO power (~5 dBm on-chip) was used. The on-chip signal power was -2.5 dBm. The transimpedance of the TIA was tuned to achieve optimal bit error rate (BER) performance for the given data rate (28 Gbaud) by trading off a lower gain (R_F=133 Ω) for a higher bandwidth. The reverse bias of 2 V for the balanced photodiodes (1 V per diode) was set though the TIA. The BER as a function of OSNR for 28 Gbaud QPSK is shown in Figure 10(a), together with two representative constellation diagrams. The transmission is below the FEC-limit (i.e. $3.8\text{x}10^{-3}$ at 7% overhead) for an OSNR of 12 dB/0.1 nm. The OSNR penalty with respect to the theoretical minimum is less than 2.5 dB. For 28 Gbaud 16-QAM our measurements are being limited by the performance of the DACs on the transmitter side. The minimal obtainable BER for this constellation using a commercial coherent receiver (picometrix), used as benchmark for the system, saturated around $2\text{x}10^{-5}$. Nevertheless, below FEC threshold operation was realized, as shown in Figure 10(b) and 10(c) together with a representative constellation diagram. In Figure 10(b) the LO power (in fiber) is swept for a constant signal power (4.5 dBm in fiber), while the signal power is swept for a constant LO-power (14.7 dBm in fiber) in Figure 10(c). A regime of below FEC operation is obtained. In both curves the error rate increases again after a certain input power, indicating possible degeneration of the transimpedance amplifier due to high input current or saturation of the photodiodes due to the high optical input power.

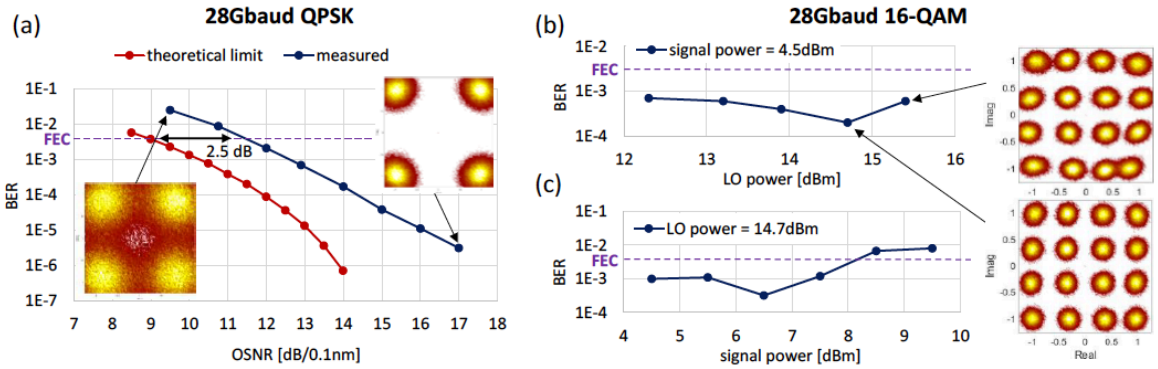

Figure 10: (a) BER versus OSNR curve for 28 Gbaud QPSK; (b) 28 Gbaud 16-QAM BER versus LO power together with representative constellation diagrams illustrating the BER degradation at higher LO power; (c) 28 Gbaud 16-QAM BER versus signal power. Below FEC operation is obtained.

In the experiment at 28Gbaud, the 2-channel TIA array consumes about 120 mA from the 2.5V supply (both for QPSK and 16-QAM operation), yielding a low overall power consumption of 155 mW per TIA, a factor of three lower than in [15] and a factor of 1.6 lower compared to [16].

5. Conclusions

An ultra-compact silicon photonic coherent receiver (0.3 mm by 0.7 mm) integrated with a 0.13-μm SiGe BiCMOS transimpedance amplifier with low power consumption (155 mW/channel) is demonstrated in this paper. Operation below FEC threshold for QPSK and 16-QAM at 28 Gbaud is obtained. This demonstration paves the way for the realization of low-power, low-cost and ultra-compact silicon photonic coherent transceivers for optical access network applications, using this coherent receiver design and an EAM-based transmitter. Potentially, a III-V-on-silicon narrow linewidth laser source can be integrated (serving as local oscillator and transmitter laser) as recently demonstrated in [25].

Acknowledgements

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