

Invited Paper

The 40 Gbps Cascaded Bit-interleaving PON

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Abstract

In this paper, a 40 Gbps cascaded bit-interleaving passive optical network (CBI-PON) is proposed to achieve power reduction in the network. The massive number of devices in the access network make that power consumption reduction in this part of the network has a major impact on the total network power consumption. Starting from the proven BiPON technology, an extension to this concept is proposed to introduce multiple levels of bit-interleaving. The paper discusses the CBI protocol in detail, as well as an ASIC implementation of the required custom CBI Repeater and End-ONT. From the measurements of this first 40 Gbps ASIC prototype, power consumption reduction estimates are presented.

Keywords: BiPON, CBI, Cascaded, 40 Gbps, PON

1. Introduction

When the World Wide Web was first introduced in the 1990s, a minimal range of services was offered to a very limited set of end users. However, since then the number of services has vastly increased, as has the number of end users [1]. These two factors have led to an ever-increasing demand for higher bandwidth, causing the data rates in the access networks to rise very quickly. Along with these rising data rates, the power consumption of the numerous optical network units (ONUs) has increased. Today, the Internet accounts for about 10% [2] of the global power consumption. It is clear that a large contribution like this

has a significant environmental impact [3, 4]. The emergence of new technologies such as the move to the cloud and the Internet of Things, along with a list of developing countries where the number of internet connections is strongly rising, assure a growth in the demand for higher bandwidth in the foreseeable future. Together with this increase, the importance of its effects on the environment grows massively. In order to sustain the welfare people have gotten used to in the developed world, we will have to find ways to reduce the pressure our society is putting on the earth and its resources. One of these ways is trying to significantly reduce the power consumption of the Internet, due to its large contribution to the global power consumption. An example of these efforts is the bit-interleaving passive optical network (BiPON) protocol, introduced in [5, 6] in the context of GreenTouch. This was a radical paradigm-shift from the current dogmatic use of packet-based communication, demonstrating a massive reduction on the power consumption. A BiPON ONU ASIC was designed and implemented [7], resulting in a 10 Gbps system which demonstrated a power saving factor from 35 to 180,

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depending on the downstream rate [6].

In this paper, we propose the 40 Gbps BiPON protocol, accommodating the need for a $4\times$ data rate increase, while achieving a low power consumption. Additionally, we introduce the cascaded bit-interleaving PON (CBI-PON) concept [8, 9, 10]: applying the bit-interleaving technique on different levels throughout the access network to reduce the power consumption even more.

Section 2 starts by explaining the concept of a bit-interleaving PON (as introduced in [7, 6]) as an alternative to the traditional packet-based PON. In section 3 an elaborated explanation of the cascaded extension of BiPON, CBI-PON, is given. Section 4 focuses on the 40 Gbps implementation of the CBI-PON protocol, whereas section 5 discusses the required analog front-end. In section 6 the digital processing in the 40 Gbps CBI-PON network devices is explained. Section 7 introduces the 40 Gbps ASIC implementation named CABINET. The power consumption reduction is addressed in section 8, followed by the conclusion in section 9.

2. Bit-interleaving Passive Optical Network

2.1. Packet-based Time Division Multiplexing

A traditional PON uses time division multiplexing (TDM) to allow the optical line terminal (OLT) to reach multiple ONUs on a shared optical fiber. In this scenario, each ONU is appointed a time slot in which this ONU receives a designated data packet, avoiding collision problems. However, all data sent from the OLT reaches every ONU, which then has to process all this data to extract the useful data and discard all data destined for other ONUs. This is shown schematically in Figure 1.

2.2. Bit-based Time Division Multiplexing

An alternative approach to packet-based time division multiplexing is to reduce the appointed time slots to 1 bit instead of 1 packet. Every successive bit is therefore intended for a different ONU. This is illustrated in Figure 2.

Compared to packet-based TDM, bit-based TDM requires a modified OLT to send the data in a bit-interleaved fashion and modified ONUs to correctly interpret the incoming data.

2.3. Receiver architecture comparison

We consider XG-PON [11] as an example of a packet-based TDM implementation of a PON. A typical XG-PON receiver has an architecture as depicted in Figure 3.

From this architecture it is apparent that the major drawback of using packet-based TDM is its lack of power efficiency. It is not until the XGEM stage that unneeded data is discarded and the receiver can start operating at the user rate instead of the full line rate. Since power consumption scales with the processing speed, the circuits operating at the full line rate clearly raise the total power consumption.

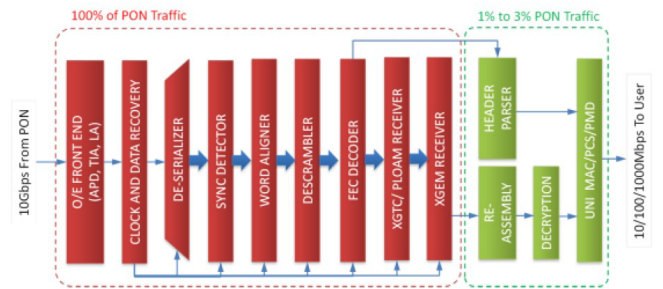


Figure 3: XG-PON Receiver Architecture [5, 12]

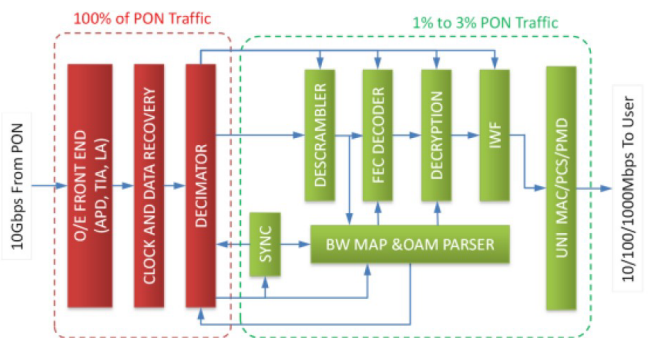


Figure 4: BiPON Receiver Architecture [5, 12]

The bit-interleaving PON (BiPON) implements a bit-based TDM. As a result, the receiver architecture used in

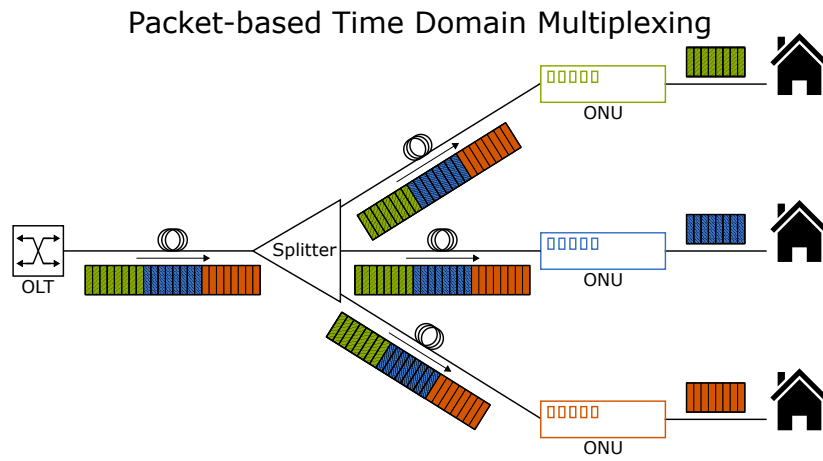


Figure 1: Packet-based Time Division Multiplexing PON

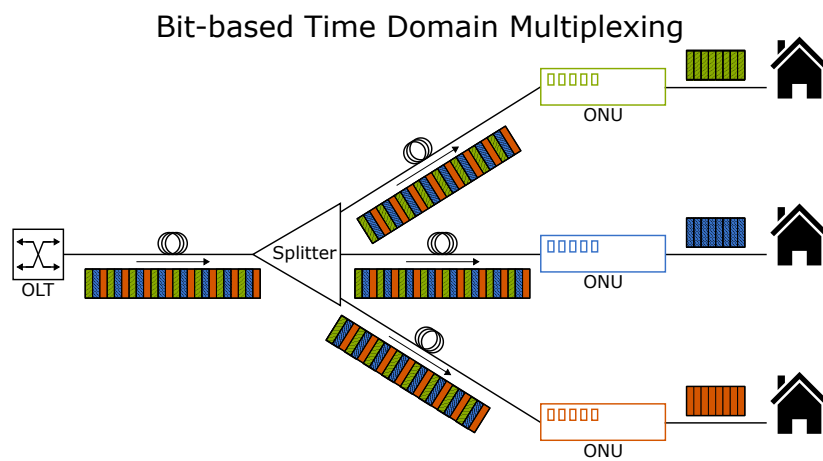


Figure 2: Bit-based Time Division Multiplexing PON

BiPON shows a completely different picture. Due to the bit-interleaving, an ONU receiver can very easily discard¹²⁵ unneeded data by a simple decimation operation. This⁹⁰ decimation can happen very early in the receiving flow, and therefore reduces the number of circuits required to operate at full line rate, as is shown in Figure 4. Since the majority of the circuits in the BiPON receiver archi-¹³⁰ tecture operate at the much lower user rate, the power consumption drops considerably.⁹⁵

2.4. BiPON Frame

In BiPON, data is organized in custom BiPON frames having 2 parts: a header and a payload. The header¹³⁵ is a fixed-rate (1/256 of the line rate) section used for protocol-specific information such as the synchronization word, ONU ID, DS/US bandwidth map and OAM data. This provides BiPON with the property of dynamic bandwidth allocation, a feature that is much needed with the¹⁴⁰ uprising of different new internet services. The BiPON frame header is composed of several header ‘lanes’. Each of these lanes contains the receiver settings, i.e. the user rate and payload offset, for an ONU with a particular ID. These settings are used to adjust the receiver hardware to¹⁴⁵ sample the payload bits that are destined for that specific receiver.¹¹⁰

3. Cascaded BiPON - CBI-PON

In BiPON, the bit-interleaving is only applied at the¹⁵⁰ level of the access network, where the leaf nodes are custom ONUs. We propose a cascaded BiPON (CBI-PON) that¹¹⁵ goes beyond the borders of the access networks and brings the BiPON concept to the metro/edge network. Figure 6 depicts the cascaded BiPON network architecture.¹⁵⁵

Alongside the development of the End-ONTs (Optical¹²⁰ Network Terminal), serving as the leaf nodes for the access network, the need for repeaters to connect different PON levels arises.

During the development of the CBI-PON, a 3-level PON was assumed in order to retain sane end-user speeds. Even though the development of CBI-PON was done for a 3-level PON, the concept is scalable to any number of levels. Every level has a maximum downstream line rate which is 1/4 of its parent level. The upstream line rate is always 1/4 of the downstream line rate.

3.1. CBI Levels and Devices

The primary level L1 is a metro/edge network that consolidates traffic from the core network, other metro/edge networks and access networks. On this primary level, we find L1 CBI Repeaters (R1) and L1 CBI End-ONTs (N1). R1 selects traffic from the primary CBI-PON and delivers it to a secondary level or access PON.

Next to the CBI Repeaters and CBI End-ONTs, there is one CBI Interleaver (CBI-I) in the primary level PON. It serves as the gateway between the CBI-PON domain and the core network or another metro/edge network. Downstream traffic from outside of the CBI-PON arrives at the CBI-I which then schedules the traffic and composes the primary CBI downstream (DS) frames.

On the secondary level, we find L2 CBI Repeaters (R2) and L2 CBI End-ONTs (N2). Similarly to R1, R2 selects traffic from the secondary CBI-PON and delivers it to a tertiary level or Home PON. The tertiary level is the lowest level, and is therefore only comprised of L3 CBI End-ONTs (N3).

3.2. CBI Frame

As in BiPON, data traffic is organized in a custom frame. Due to the multi-level architecture, this custom frame is more complex than was the case in BiPON. At each level, the CBI frame still consist of a header and a payload. The header has three subsections: a SYNC, an RNID and a BWMAP, and is composed of several header ‘lanes’. The number of lanes is dependent on the CBI level

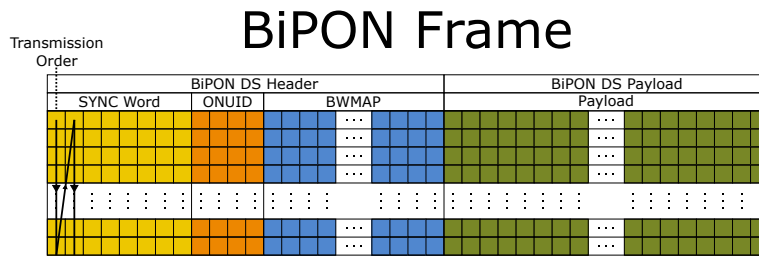


Figure 5: BiPON Frame Structure

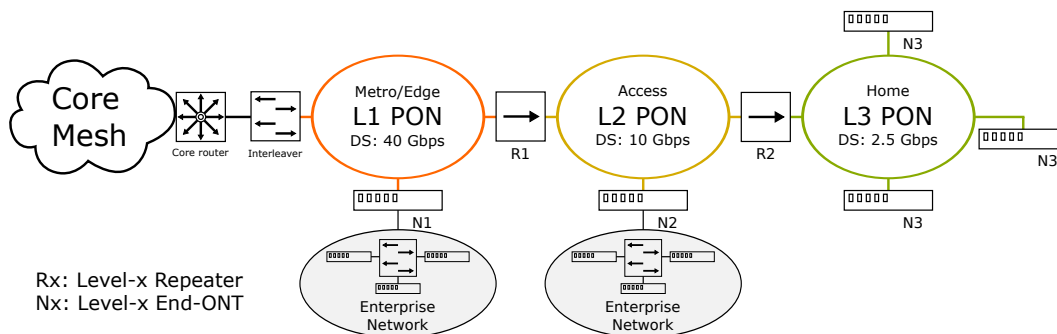


Figure 6: Cascaded Bit-Interleaving PON Network Architecture

160 and the rate.

For a primary level (L1) CBI frame, the payload determined by a particular header lane is either an L2 CBI frame (to be forwarded by an L1 Repeater) or L1 end-user data (to be received by an L1 End-ONT).
 165

Similarly, for a secondary level (L2) CBI frame, the payload belonging to a header lane is either an L3 CBI frame (to be forwarded by an L2 Repeater) or L2 end-user data (to be received by an L2 End-ONT).
 170

Finally, the payload in an L3 CBI frame lane is always L3 end-user data (to be received by an L3 End-ONT). The CBI frame structure is illustrated in Figure 7.
 175

The frame length is kept constant throughout all CBI-PON levels and equals 125 us. To achieve this constant frame length, the number of header lanes and the payload

sizes of L2 and L3 CBI-PON frames scale proportionally with the input line rate.
 180

4. 40 Gbps CBI-PON Implementation

As a proof-of-concept, a 40 Gbps CBI-PON was implemented. Table 1 shows the line rates chosen for the multiple levels to accommodate a 40 Gbps CBI-PON, and how the number of header lanes and payload sizes vary according to the line rate in order to maintain a 125 us frame length. Figure 8 shows a CBI frame with its L1, L2 and L3 implementations for the 40 Gbps demonstrator.

As mentioned in section 3, we need a CBI Interleaver, CBI Repeaters (L1 and L2) and CBI End-ONTs (L1, L2 and L3) to realize a CBI-PON. In the following paragraphs, the implementation of these devices is discussed.

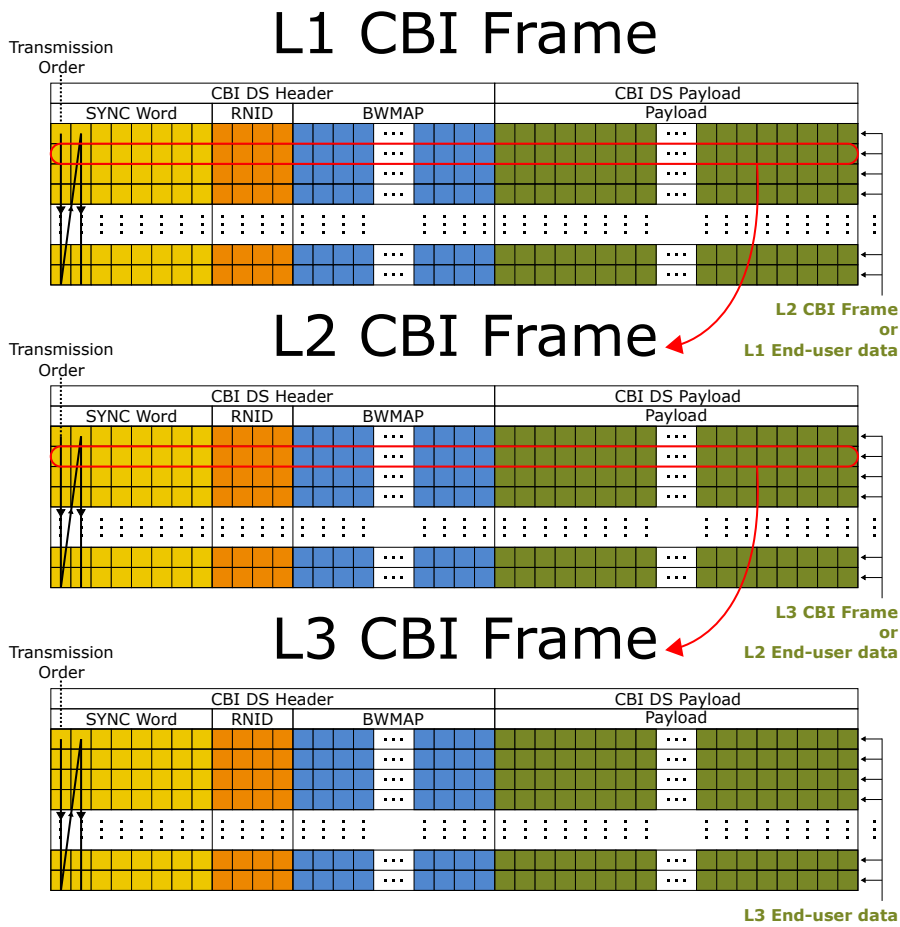


Figure 7: CBI Frame Structure

	Primary (L1)	Secondary (L2)				Tertiary (L3)			
Rate (Gbps)	40	10	5	2.5	1.25	2.5	1.25	0.625	0.3125
# Header lanes	1024	256	128	64	32	64	32	16	8
Payload length (octets)	606208	151552	75776	37888	18944	37888	18944	9472	4736
Frame length (octets)	622080	155520	77760	38880	19440	38880	19440	9720	4860
Frame time (us)	125	125	125	125	125	125	125	125	125

Table 1: 40 Gbps frame time calculation

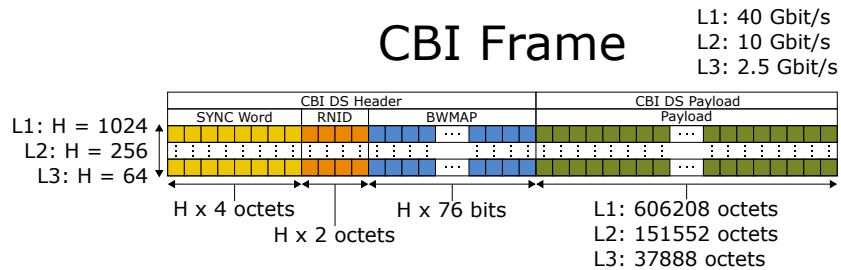


Figure 8: 40 Gbps CBI Frame

4.1. CBI Interleaver

The CBI Interleaver acts as the bridge between the core network and the CBI-PON domain. It was implemented on an FPGA board with 4 10 Gbps transceivers, followed by a 4:1 multiplexer (MUX) creating the required 40 Gbps data stream. A laser diode (LD) followed by a transmitter optical sub-assembly (TOSA) is used to create the optical signal. Figure 9 shows the schematic overview of the CBI Interleaver.

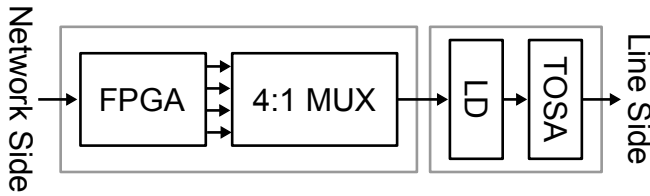


Figure 9: CBI Interleaver

4.2. CBI Repeater

As shown in Figure 10, the CBI Repeater uses a custom multi-rate IC (CABINET) to support L1 and L2 CBI operation. Using a receiver optical sub-assembly (ROSA) followed by a trans-impedance amplifier (TIA) combined with a limiting amplifier (LA), the optical signal from the PON is converted to electrical levels and used as the input for the CABINET ASIC. After the data recovery (DS CDR), the repeater digital processing extracts the correct bits to be sent to the lower level PON and is sent using a LD followed by a TOSA.

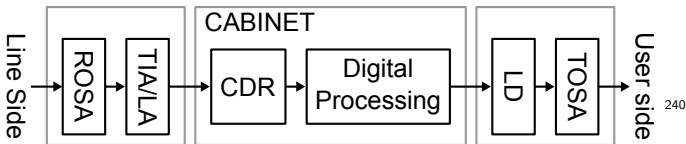


Figure 10: CBI Repeater

4.3. CBI End-ONT

The CBI End-ONT uses the same custom IC (CABINET) to support L1, L2 and L3 CBI operation. Like the

CBI Repeater, a ROSA followed by a TIA combined with an LA converts the optical input signal from the PON to electrical levels, which is sent to the CABINET. Following the data recovery is the End-ONT digital processing, extracting the data which is sent to the FPGA that provides a standard Ethernet interface to the end user. This system is illustrated in Figure 11.

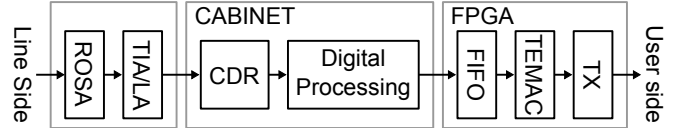


Figure 11: CBI End-ONT

4.4. CABINET ASIC

As mentioned in the previous paragraphs, a custom ASIC was required to implement the CBI Repeater and End-ONT. Therefore, we developed the CABINET ASIC: a multi-mode, multi-rate chip supporting both repeater and End-ONT mode operation at rates corresponding to the primary (L1), secondary (L2) and tertiary (L3) level. The CABINET IC is composed of two large blocks: (1) a 40 Gbps analog front-end and (2) a CBI frame processing block. In the following sections, we will discuss each of these blocks in more detail.

5. 40 Gbps Analog Front-End: Sub-Sampling CDR

Figure 12 shows a schematic block diagram of the analog front-end in the CABINET ASIC, which consists mainly of a clock-and-data recovery circuit (CDR). This circuit is indispensable to receive the data, since the on-chip sampling clock is not synchronized with the incoming data. Therefore, the sampling clock should be phase-aligned with the incoming data to assure correct sampling. The clock-and-data recovery circuit uses the transitions of the incoming data to achieve this phase-alignment.

The CDR architecture used is a typical charge pump (CP) CDR using a 2x oversampling bang-bang phase detector (BB-PD) and a second order loop filter [13, 14]. It

is however a 1:4 sub-sampling CDR. This means that only 1 out of 4 bits is recovered from a 40 Gbps input stream, because the decimation rate in the CBI protocol is at least 1:4.

This sub-sampling simplifies the CDR building blocks and decreases power consumption by reducing the operating frequency. In such systems, there are two critical blocks: the sampling stage and the voltage-controlled oscillator (VCO).

5.1. Sampling stage

The sampling stage of the CDR uses 1:4 sub-samplers. Each sampler is a flip-flop designed to have a short setup and hold time, so it can handle up to 40 Gbps input data while sampling at 10 Gbps, effectively resulting in a 1:4 sub-sampling operation.

Three samplers are used to retrieve the necessary phase information from the input data, driven by 3 adjacent clock phases generated by the VCO, as depicted on Figure 13. Sampling with these clock phases results in 3 bit values: a, b and c. These are needed to determine the early/late signal based on a transition in the input data.

5.2. Phase Detector Logic Core

In order to sample both a and c in the center of the bit, the bits from the sampling stage are compared to decide whether the clock is early or late. For example, if a and b are equal, but different from c: b is sampled around the transition, but since we sampled the same value as the previous bit, the transition has not occurred yet. This implies that the clock is early. On the other hand, if b and c are equal, but different from a, the clock is late. This gives us enough information to adjust the clock phase. This is summarized in Figure 14.

5.3. 8-phase 10 GHz Voltage-Controlled Oscillator

Even though only a 10 GHz clock is needed, we need 8 phases of this clock to be able to sub-sample the correct bit out of the incoming 40 Gbps data. Today, there are two

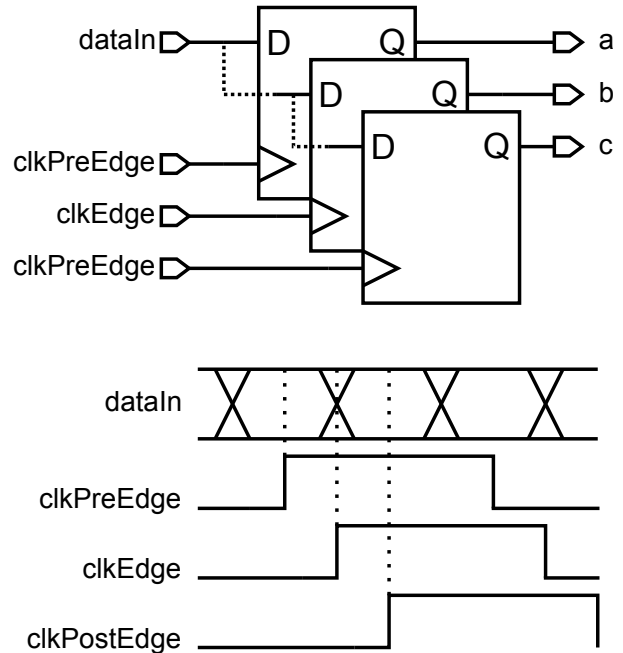
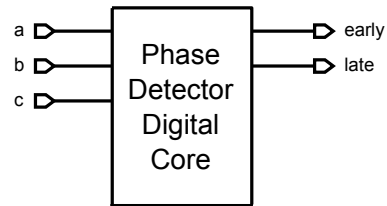


Figure 13: Sampling Stage



a	b	c	early	late
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	0	1
1	0	1	0	0
1	1	0	1	0
1	1	1	0	0

Figure 14: Phase Detector

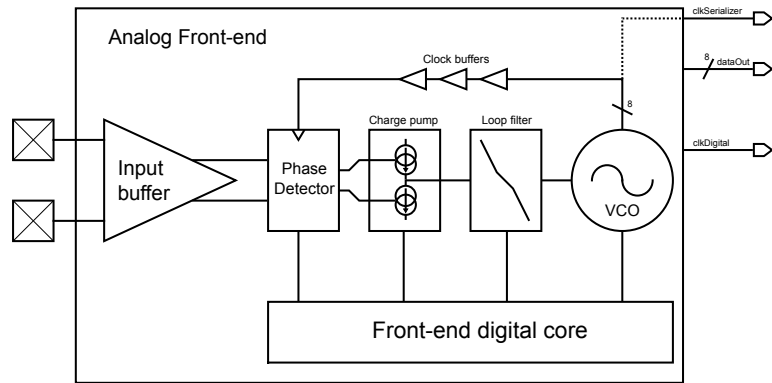


Figure 12: CABINET ASIC Analog Front-End Block Diagram

major oscillator architectures in use: ring oscillator and
 285 LC oscillators. LC oscillators, despite offering a superior
 phase noise, exhibit a limited tuning range and consume a
 lot of chip area due to the presence of an inductor. Their
 counterpart, ring oscillators, do not perform very well with
 respect to phase noise, but are very small and have large
 290 tuning ranges [15]. Additionally, thanks to their architec-
 ture, they supply multiple phases of the oscillating signal,
 which makes them ideal for this system.

A ring oscillator is a chain of delay cells (stages) con-
 295 nected in a ring-like structure. To achieve oscillation in
 this structure, the Barkhausen criterion [16, 17, 18] should
 be satisfied. These oscillators can be either single-ended
 or differential. Due to the Barkhausen criterion, single-
 ended oscillators can only be composed of an odd number
 300 of stages N , which is the number of stages a single-ended
 oscillator supplies. On the other hand, differential oscil-
 lators can employ an even number of stages, and supply
 $2N$ phases. Since the voltage-controlled oscillator has to
 supply 8 phases, a 4-stage differential ring oscillator was
 305 used, shown in Figure 15.

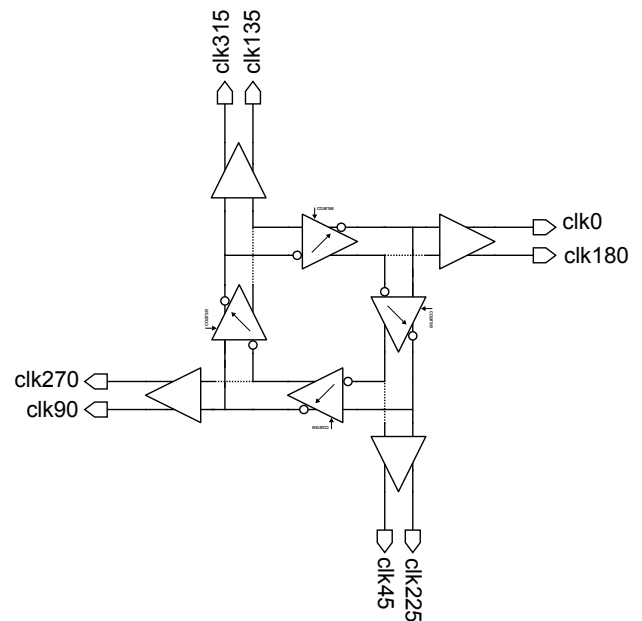


Figure 15: 8-Phase 10 GHz Voltage-Controlled Oscillator

6. CBI Frame Processing

In this section, we discuss the digital processing required for the CBI protocol. Once the clock and data have been recovered, the received frame data has to be interpreted. As a first step, common to both CBI Repeater and End-ONT, a synchronization procedure should be followed. Following synchronization, the payload data is treated depending on the receiver being a CBI Repeater or an End-ONT.

6.1. Synchronization procedure

During the synchronization procedure the header data of the incoming frame is sampled and a search for the SYNC word is performed. Once it has been found, the header lane offset is calculated based on the difference between the received ONU ID and the device's ONU ID. This procedure is shown in Figure 16. Once synchronization is achieved, the header data can be processed.

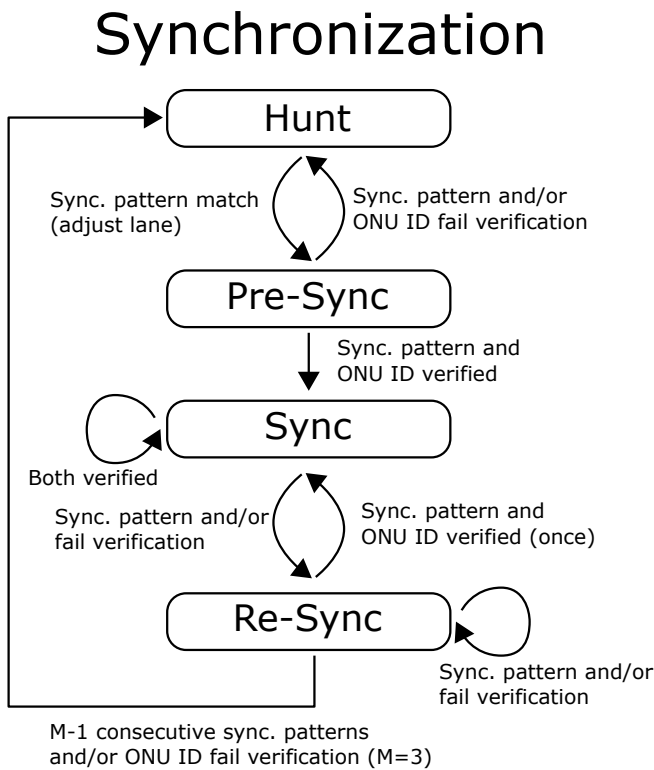


Figure 16: Synchronization Procedure

6.2. Repeater

In repeater mode, the header data is descrambled to obtain the bandwidth map (BWMAP), which is then parsed to get the necessary parameters about the link rate. The payload of incoming frames is then forwarded to the output without any further processing. For every next frame received, the BWMAP is monitored for changes. This flow is depicted in Figure 17.

6.3. End-ONT

In End-ONT mode, like in repeater mode, the BWMAP is retrieved from the descrambled header data. The link rate from the BWMAP determines the selection of the correct payload clock. Since the CDR data is already sub-sampled, the CDR sampling channel is adjusted to the correct channel if necessary (determined by the offset value in the BWMAP). Subsequently, the payload clock is used to sample the payload data, which is then descrambled and sent to the output of the chip. The End-ONT flow is also shown in Figure 17.

7. CABINET ASIC Implementation

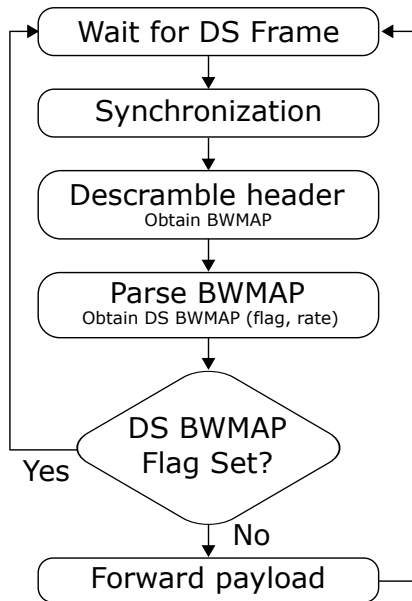
The CABINET ASIC as described was implemented in a 40 nm low power CMOS technology. The full layout of the ASIC is shown in Figure 18, while a picture of the fabricated die is shown in Figure 19.

8. Power Consumption Reduction Estimates

Due to some issues with the first prototype of the CABINET ASIC, not all modes were completely functional. However, based on the simulated power consumption and the working parts of the ASIC, the total power consumption of the ASIC could be extrapolated, the results of which are presented in Table 8.

Considering an L1 Repeater, we find the power estimate to be 187.63 mW. Looking at a 2.5G PONs, the average number of ONUs per PON is 73.36, which results

Repeater



End-ONT

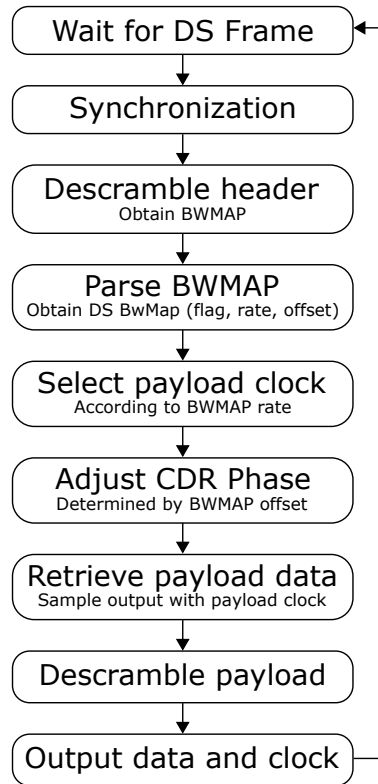


Figure 17: Repeater and End-ONT Processing

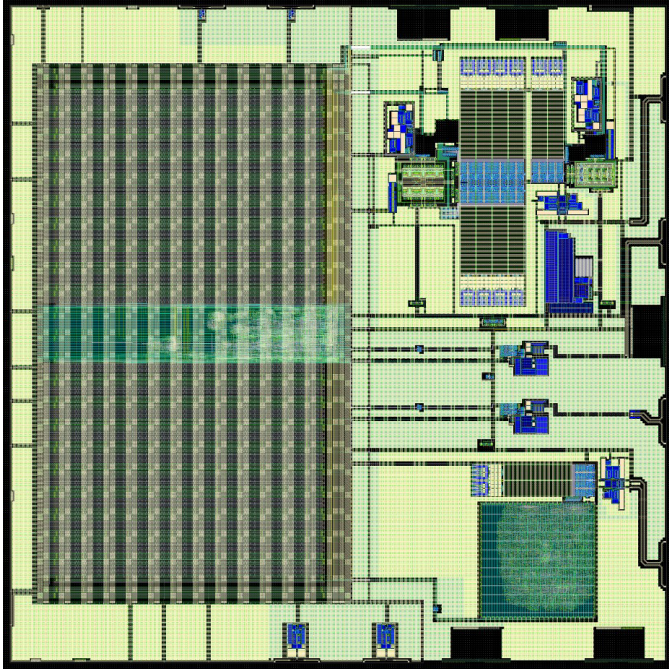


Figure 18: CABINET ASIC Layout

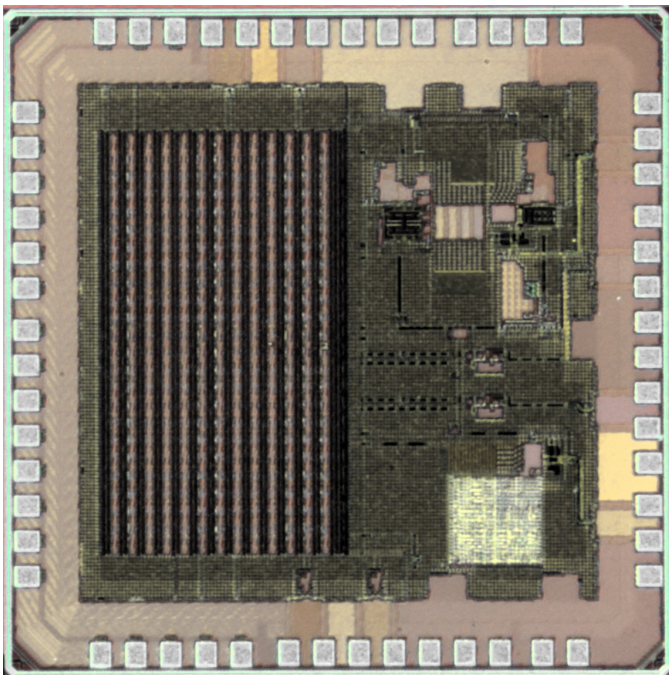


Figure 19: CABINET ASIC Die Photo

CBI Repeater		
	Simulated (mW)	Extrapolated (mW)
L1	126	187.63
L2	86.5	120.48

CBI End-ONT		
	Simulated (mW)	Extrapolated (mW)
L1	106	162.55
L2	66.5	94.55
L3	50.88	61.94

Table 2: Extrapolated CABINET Power Consumption

in a power estimate per ONU of 2.56 mW for the L1 repeater. When compared to an aggregation switch in 2010, consuming 201 mW per ONU, this amounts to a power reduction factor of 80x.

Regarding the digital processing in the ONU, we can estimate this as being the digital processing of an L2 repeater combined with 2 L3 End-ONTs. The power consumption of this system is estimated to be 241.5 mW. In 2010, the power consumption of the digital processing per ONU was 1.481 W, which translates to a 6x power reduction estimate.

More importantly, we can evaluate the power consumption in the network by comparing the state-of-the-art solution with our proposed solution.

8.1. State-of-the-art solution

The state-of-the-art solution is a combination of Ethernet metro/edge networks and GPON access networks. From the Cisco product brief, we can estimate the power consumption of a 2x10GE line card at 370 W, while a 1GE GPON OLT port consumes about 11 W. Power consumption of a GPON ONU is estimated at 6.5 W. A small access fiber-to-the-home (FTTH) deployment with 768 single family units (SFUs) requires 2 times a 2x10GE line card and, assuming a 32 split, 24 GPON OLT ports and 768 SFU GPON ONTs. The power consumption of this

deployment is therefore estimated to be 5996 W.

8.2. Proposed solution

Replacing the state-of-the-art solution with a CBI-PON, by using a CBI Interleaver as a line card, a CBI Repeater for every GPON OLT port and replacing the GPON ONTs with CBI EndONTs, we can calculate the power reduction that is to be expected when using a CBI-PON.

The CBI Interleaver power consumption is assumed to be around 15 W, based on the estimates of the FPGA (9 W), the MUX (2 W) and the optics (4 W).

The CBI Repeater is estimated at 5 W, mainly due to the optical-electrical (O/E) and electrical-optical (E/O) conversions, since the CABINET ASIC was estimated at less than 200 mW. Similarly, the CBI End-ONT power consumption accounts for 3 W, also dominated by the O/E and E/O conversions.

$$15W + 24 \times 5W + 768 \times 3W = 2439W$$

With these numbers, the total network power consumption estimate for the CBI-PON becomes 2439 W.

8.3. Power reduction estimate

The state-of-the-art solution consumes a total of 5996 W, while the proposed CBI-PON solution only consumes 2439 W, which is an estimated power reduction of around 60%.

9. Conclusion

In this paper, we have proposed the 40 Gbps cascaded bit-interleaving PON as an extension on the BiPON introduced in [5, 6]. The CBI Repeater and CBI End-ONT implementations were introduced, together with the multi-rate, multi-mode CABINET ASIC implementation. The critical building blocks for the CABINET ASIC were discussed, followed by the CBI frame processing.

Finally, a power consumption estimate of the full network was made for a state-of-the-art solution and for the proposed CBI-PON, showing a power reduction of about 60%, from 5996 W to 2439 W for a small FTTH access network with 768 ONUs.

10. Acknowledgement

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