A 64 Gb/s PAM-4 Linear Optical Receiver

Bart Moeneclaey¹, Giannis Kanakis², Jochen Verbrugghe¹, Nikos Iliadis², Wouter Soenen¹, Dimitrios Kalavrouziotis², Christos Spatharakis², Stefanos Dris², Xin Yin¹, Paraskevas Bakopoulos², Elad Mentovich³, Hercules Avramopoulos², Johan Bauwelinck¹

¹INTEC/IMEC, Ghent University, Sint-Pietersnieuwstraat 41, 9000 Ghent, Belgium

²School of Electrical & Computer Engineering, National Technical University of Athens, Iroon Polytechniou 9, 15780 Athens, Greece

³Mellanox Technologies, Hakidma 26, Yokneam 2069200, Israel

Author e-mail address: bart.moeneclaey@intec.ugent.be

Abstract: We present a linear optical receiver realized on 130 nm SiGe BiCMOS. Error-free operation assuming FEC is shown at bitrates up to 64 Gb/s (32 Gbaud) with 165 mW power consumption, corresponding to 2.578 pJ/bit.

OCIS codes: (200.4650) Optical interconnects; (060.2380) Fiber optics sources and detectors; (230.0250) Optoelectronics.

1. Introduction

Cloud services, video applications and sensor networks are causing datacenter traffic to soar at a 25% annual pace. These enormous capacity requirements are pushing serial line rates of optical interconnects beyond 25 Gb/s (offered by current premium-grade products), with roadmaps and ongoing standardization efforts aiming at 39-56 Gb/s per data lane (e.g. Optical Internetworking Forum, Infiniband Trade Association). Scaling the serial line rate is pivotal not only for upgrading aggregate link capacity of the optical interconnect but also for increasing front-panel I/O density of the datacenter switch, which currently represents a daunting obstacle towards upgrading switch throughput. In this context, serial optical links have been realized at line rates up to 64 Gb/s with NRZ signaling, being the simplest and most common format in Datacom [1]. To achieve this performance, equalization was employed to compensate the bandwidth limitation of the 26 GHz VCSEL. Although of proven feasibility, this approach raises a number of concerns regarding power consumption of the equalizer, integrity of the high speed electrical signal propagating from the ASIC to the optical transceiver module as well as optical reach limitations due to fiber dispersion. As an alternative, PAM-4 signaling relaxes the requirements for equalization (and associated power consumption) and is more tolerant to transmission penalties such as dispersion and jitter [2]. Compared to other advanced modulation formats, PAM-4 is simpler to implement and has a precedent in standardization (IEEE 802.3bj). However, these virtues of PAM-4 come at the cost of increased linearity requirements for the transmitter and receiver subsystems.

A number of linear optical receivers suited for 40 Gb/s PAM-4 operation have been reported in the literature on various technology platforms such as 130 nm SiGe BiCMOS [3], 180 nm CMOS [4], 90 nm CMOS [5], 65 nm CMOS [6] and 28 nm CMOS [7]. Further scaling of the linear receiver speed is an outright challenge that involves design tradeoffs between bandwidth, gain, linearity, power consumption and noise. In this work we present a linear optical receiver realized on 130 nm SiGe BiCMOS technology, operating with PAM-4 signals at line rates ranging from 50 to 64 Gb/s, achieving the fastest PAM-4 performance reported so far to our knowledge. The receiver has been developed for single-mode links, avoiding the bandwidth-distance product limitation of multimode fiber and offering a viable solution when longer reach is required, e.g. in mega-datacenters [8] or in optically-switched flexible datacenter architectures [9].

2. Linear Receiver Architecture

Fig. 1(a) shows a simplified block diagram of the linear receiver and photodiode array. The receiver consists of two

Fig.1. (a) Block diagram and (b) die micrograph of the linear receiver.

identical channels. However, only one is considered in this paper. The photodiodes have a responsivity (including coupling loss) of 0.44 A/W. The data path contains a transimpedance amplifier (TIA) input stage, a linear main amplifier and a linear output stage. The TIA input stage provides a low-impedance input for the photocurrent with its shunt-shunt feedback amplifier topology. The feedback resistor is implemented as an nMOS transistor biased in the linear region in order to control the transimpedance gain. The output voltage of this stage is applied to the non-inverting input of the main amplifier, consisting of three fully differential gain stages. The output stage drives the 100 Ω differential load impedance. The three gain stages and the output driver utilize a differential pair degenerated by an nMOS transistor biased in the linear region in order to control the gain. A control loop is formed using the balancing error amplifier, which removes the dc-offset between both output signals by adjusting the dc-voltage at the inverting input of the main amplifier. The die core is powered by a 2.5 V supply and draws 66 mA per channel.

The linear was produced in a 130 nm SiGe BiCMOS process technology. A micrograph of the die, wire-bonded to the photodiode array, is presented in Fig. 1(b). The total chip area is 3000 $\mu\text{m} \times 900 \mu\text{m}$, with each channel occupying 1100 $\mu\text{m} \times 900 \mu\text{m}$.

3. Experimental Setup

Fig. 2 shows the experimental setup for the evaluation of the linear receiver at 25, 28 and 32 Gbaud. The NRZ tributaries used to generate the PAM-4 test signal were produced by a Centellax TG1P4A pulse pattern generator (PPG), phase-locked at half rate to an Anritsu MG3694B signal generator. The complementary NRZ outputs of the PPG were de-correlated by means of coaxial cables of unequal length for each signal path. The PPG outputs were fed into the respective inputs of a 40-Gb/s-capable Ti:LiNbO₃ Dual-Drive Mach-Zehnder Modulator (MZM), serving as the MSB and LSB input pseudorandom bit sequence (PRBS). Two Centellax OA5MVM broadband amplifiers were used to adjust the input power levels of the MSB and LSB data streams before entering the MZM. In order to generate an optical PAM-4 signal at the MZM, the voltage swing was set to approximately $2/3 \cdot V_\pi$ and $2/3 \cdot V_\pi$ for the MSB and LSB data stream, respectively. An electrical phase shifter was employed in one data path for precise synchronization of the input electrical data streams in the MZM. A Distributed-Feedback (DFB) laser emitting 13 dBm at 1550 nm provided the optical carrier for the MZM. The MZM output PAM-4 optical signal was then fed into the linear receiver through a cleaved SMF fiber using a vertical probing arrangement. A variable optical attenuator was used to adjust the incident optical power in the linear receiver for BER measurements. The receiver output was observed with an Agilent Infinium DCA-J 86100C equivalent-time oscilloscope whereas BER measurements were obtained after acquisition of both differential outputs of the received PAM-4 signal with a 33GHz, 80 GSa/s Agilent Infinium DSO-X 93304 real-time oscilloscope and subsequent offline processing in order to implement the thresholding function for error counting.

4. Results and Discussion

The receiver was evaluated at 25, 28 and 32 Gbaud. The electrical eye diagrams, acquired with the equivalent-time oscilloscope, are shown in Fig. 3(a-c), while the distribution of PAM-4 symbols is depicted in the respective histograms of Fig. 3(d-e), after signal acquisition in the real-time oscilloscope, offline clock recovery and re-sampling. It can be observed that even though receiver performance gradually deteriorates with increasing baud rate, the eye diagram is still quite open up to 32 Gbaud, whereas the clear separation of the symbol distributions in the corresponding histograms implies sufficient reception performance.

The PAM-4 optical signal generated by operating the MZM with unequal amplitudes for the MSB and LSB tributaries exhibited an extinction ratio (ER) of about 20 dB, while the power consumption of the TIA after optimizing the receiver settings for the aforementioned input ER was 165 mW, yielding an energy consumption of

Fig.2. Experimental Setup for the evaluation of the Linear Receiver at 25, 28 and 32 Gbaud.

Fig.3. Receiver output signal eye diagrams at (a) 25, (b) 28 and (c) 32 Gbaud as observed on the equivalent-time oscilloscope; symbol histograms at (d) 25, (e) 28 and (f) 32 Gbaud acquired by the real-time oscilloscope and BER bathtubs estimated after signal digitization, offline clock recovery, re-sampling and automatic thresholding for symbol detection.

2.578 pJ/bit at 64 Gb/s.

Bit-error-rate (BER) measurements were performed to the digitized signal at the real-time oscilloscope after offline clock recovery, re-sampling and automatic thresholding for symbol detection, assuming Gray encoding. The BER performance was assessed by comparing the received sampled signal to the original bit sequence and counting the actual symbol errors that occurred during reception. It should be noted that the limited data acquisition capacity of the real-time oscilloscope (1.28×10^7 bits at 25 Gbaud) posed a corresponding limit to the lowest measurable BER. Fig. 3(g) presents the measured bathtub curves for 25, 28 and 32 Gbaud input signals plotted against the average received optical power, derived from the measured photocurrent. As can be observed, at 25 Gbaud and average input power ranging between -2 dBm and 0.4 dBm, the received signal exhibits zero errors, which corresponds to an upper 95% confidence limit of 2.9×10^{-7} . It is clear that even at 32 Gbaud the minimum achieved BER lies well below the FEC limit, proving the adequate operation of the linear receiver.

4. Conclusions

We demonstrated a linear optical receiver fabricated on 130 nm SiGe BiCMOS process technology, operating at line rates of 50, 56 and 64 Gb/s with PAM-4 modulation format. The receiver consumed 165 mW, corresponding to an energy consumption of 2.578 pJ/bit at 64 Gb/s. Operation below the FEC limit was achieved in all cases, proving the suitability of this receiver for future optical interconnect standards with serial line rates above 50 Gb/s.

Acknowledgement: This work was partially supported by the European Commission through the FP7 project MIRAGE (www.ict-mirage.eu) and the Institute for the Promotion of Innovation by Science and Technology (IWT) in Flanders.

5. References

- [1] D. M. Kuchta et al., "64Gb/s Transmission over 57m MMF using an NRZ Modulated 850nm VCSEL", in Proc. OFC'14, Th.3C.2 (2014).
- [2] K. Szczerba et al., "4-PAM for High-Speed Short-Range Optical Communications" IEEE Opt. Commun. Netw. **4**, 885-894 (2012).
- [3] J. Knochenhauer, B. Sedighi and F. Ellinger, "40 Gbit/s transimpedance amplifier with high linearity range in 0.13 μ m SiGe BiCMOS", Electron. Lett., **47**(10), 605-606 (2011).
- [4] J. Jun-De and S.S.H. Hsu, "A 40-Gb/s transimpedance amplifier in 0.18- μ m CMOS Technology", IEEE J. Solid-State Circuits, **43**, 1449-1457(2008).
- [5] L. Chih-Fan and L. Shen-Iuan, "A 40Gb/s Transimpedance-AGC amplifier with 19dB DR in 90nm CMOS", in Proc. ISSCC'07 (2007), p.57.
- [6] S. Bashiri, et al. "A 40 Gb/s transimpedance amplifier in 65 nm CMOS", in Proc. IEEE ISCAS'10 (2010), pp. 757-760.
- [7] N. A. Quadir, P. D. Townsend and P. Ossieur, "An inductorless linear optical receiver for 20Gbaud/s (40Gb/s) PAM-4 modulation using 28nm CMOS", in Proc. IEEE International Symposium on Circuits and Systems (ISCAS'14), (2014), pp. 2473-2476.
- [8] D. Apostolopoulos et al., "Photonic integration enabling new multiplexing concepts in optical board-to-board and rack-to-rack interconnects", in Proc. SPIE 8991, Optical Interconnects XIV, 89910D (2014).
- [9] N. Farrington, et al., "A 10 us Hybrid Optical-Circuit/Electrical-Packet Network for Datacenters," in Proc. OFC'13, OW3H.3 (2013).