Opening Up Automatic Structural Design Space Exploration by Fixing Modular Simulation

VEERLE DESMET  SYLVAIN GIRBAL  OLIVIER TEMAM

Ghent University  Thales TRT  INRIA
Motivation

Need for systematic quantitative comparison

Average Speedup

VC(82)  TP(82)  SP(90)  Markov(97)  FVC(00)  DBCP(01)  TKVC(02)  TK(02)  CDPI(02)  CDSP(02)  TCP(03)  GHB(04)

[MICRO 2004, Gracia-Pérez et al.]
Computer Architecture Research

IDEA

FAIR COMPARISON

REPRODUCTION EXISTING TECHNIQUES

EXPLORATION
Design space exploration: need more than intuition and experience?

Multi-objectives

Time-to-market
ArchExplorer: repository + automatic exploration

Website

Server-side Infrastructure
FULLY AUTOMATIC

archexplorer.org

upload
daily update
test

database

pick design points
add results

simulation cluster
How to compare?

1. Custom simulator
2. Hardware compatibility
3. Software compatibility
4. Upload
Hardware compatibility

Instruction caches
Data caches
Branch predictors
Interconnects
Main memory
Accelerators

...
Software compatibility
Isolate the hardware block, possibly by from centralized control to distributed control.
Software compatibility

Wrapping in SystemC-based on UNISIM communication layer

Models of computation

Self-Configuration and parameters legality

get_connected_module()

get_parameter("buswidth")

buswidth=32

inCPU

buswidth=?
Case study

Memory sub-system for embedded processor

- PowerPC405
- 8 different cache modules available
- Complex hierarchies automatically explored
- Ranking designs for performance, power, energy, area,...
Accurate comparison needs compiler tuning as well
Best data cache mechanisms per area

CONCLUSIONS:
1. Contrast to Gracia-Pérez et al. [MICRO 2004]
2. No clear winner
3. Close to tuned parametric cache
Best data cache mechanisms per area

CONCLUSIONS:
1. Contrast to Gracia-Pérez et al. [MICRO 2004]
2. No clear winner
3. Close to tuned parametric cache
Composing cache hierarchies
Speedup and Energy Improvement
Check out this website:

ARCHEXPLORER.ORG
Design Space Exploration

Permanent on-line competition(s)

Participate and evaluate your own mechanisms

Ranking of available cache mechanisms

Only top points, i.e., points that are above the parametric envelope either performance-wise or energy-wise, are listed. To sort, click on column title.

<table>
<thead>
<tr>
<th>Cache Mechanism</th>
<th>Area in mm² (memory subsystem only)</th>
<th>Speedup (over PowerPC405)</th>
<th>Energy Improvement (over PowerPC405)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stride Prefetcher [8]</td>
<td>6.938</td>
<td>1.339</td>
<td>0.046</td>
</tr>
<tr>
<td>Tag Prefetcher [2]</td>
<td>7.090</td>
<td>1.339</td>
<td>0.047</td>
</tr>
<tr>
<td>Tag History Prefetcher</td>
<td>11.714</td>
<td>1.228</td>
<td>0.046</td>
</tr>
<tr>
<td>Global History Prefetcher [9]</td>
<td>8.560</td>
<td>1.227</td>
<td>0.046</td>
</tr>
<tr>
<td>Stride + Context-Directed Prefetcher [17]</td>
<td>14.609</td>
<td>1.327</td>
<td>0.148</td>
</tr>
<tr>
<td>Victim Cache</td>
<td>2.602</td>
<td>1.326</td>
<td>0.572</td>
</tr>
</tbody>
</table>
Conclusion

- Permanent open competition(s)
- Future:
  - superscalar processor
  - branch predictor repository
  - multi-cores
- Open for your ideas!
  - NoC, compiler extensions,...
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VEERLE DESMET
Ghent University

SYLVAIN GIRBAL
Thales TRT

OLIVIER TEMAM
INRIA