

Ge-on-Si and Ge-on-SOI thermo-optic phase shifters for the mid-infrared

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Abstract: Germanium-on-silicon thermo-optic phase shifters are demonstrated in the 5 μm wavelength range. Basic phase shifters require 700 mW of power for a 2π phase shift. The required power is brought down to 80 mW by complete undercut using focused ion beam. Finally an efficient thermo-optic phase shifter is demonstrated using germanium on SOI platform. A tuning power of 105 mW is achieved for Ge-on-SOI which is lowered to 16 mW for a free standing phase shifter.

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OCIS codes: (250.5300) Photonic integrated circuits, (160.6840) Thermo-optical materials, (250.7360) Waveguide modulators.

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1. Introduction

The germanium-on-silicon waveguide platform is a strong candidate for mid-ir photonic integration [1],[2]. Its CMOS compatibility, simple fabrication scheme and wide range transparency (germanium is transparent up to $14\ \mu\text{m}$) make it a compelling solution compared to other mid-ir integration platforms proposed so far [3],[4],[5]. Recent demonstrations of low loss waveguides and various photonic components such as Mach-Zehnder interferometers (MZIs) [6], arrayed waveguide gratings (AWGs) [7] and planar concave gratings (PCGs) [8] show the versatility of the Ge-on-Si waveguide platform.

Tuning of integrated optical components is of critical importance in many applications. This tuning can be achieved by utilizing thermo-optic phase shifters where heat is generated in the vicinity of the waveguide which affects the effective index of the optical mode [9],[10]. Thermo-optic phase tuning is achieved by either placing a heater on top of the waveguide which requires the deposition of an insulating layer of sufficient thickness which optically isolates the mode in the waveguide from the heater or by placing the heater on the side of the waveguide which avoids deposition of any intermediate cladding. In this paper, we describe the realization of side-integrated thermo-optic phase shifters for mid-ir photonic integrated circuits.

1.1. Design of the phase shifters

To investigate the thermo-optic phase shifters, we designed 1×2 Mach Zehnder Interferometers (MZIs) in the $5\ \mu\text{m}$ wavelength range with a fixed path length difference of $260\ \mu\text{m}$ which resulted in a free spectral range (FSR) of 25 nm. The circuits were designed for TM polarization for compatibility with quantum cascade laser integration. We designed the heaters in side heating configuration as schematically shown in Fig.1(a). The heater itself consisted of a $2\ \mu\text{m}$ wide and 100 nm high metal stack (Ti/Au or Cr/Au) placed on top of a $4\ \mu\text{m}$ wide germanium strip. The length of the heater section was varied from $70\ \mu\text{m}$ to $700\ \mu\text{m}$ in steps of $70\ \mu\text{m}$ and both the ends were connected to $100\ \mu\text{m} \times 100\ \mu\text{m}$ pads. The distance between the waveguide (etched through the $2\ \mu\text{m}$ thick Ge core layer and $2.2\ \mu\text{m}$ wide) and neighboring germanium heater was chosen to be $2\ \mu\text{m}$ which is the limit of our lithography tool. The thermal simulations were performed using COMSOL multiphysics. We performed steady state FEM 3-D simulations to calculate the temperature change as a function of dissipated power in the heater as shown in Fig.1(c) where a zoomed version of the simulation window can be seen. The substrate and the air top cladding were kept at a height of $200\ \mu\text{m}$ and at a width of $400\ \mu\text{m}$. The length of the waveguide was always kept $400\ \mu\text{m}$ additional to the length of the heater such that heat flow along the waveguide itself can be taken in account.

The temperature dependent thermo-optic coefficient of germanium was extracted from [11] for

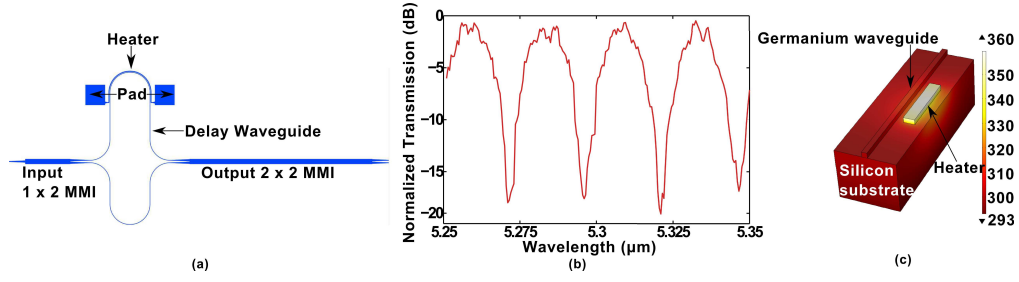


Fig. 1. (a) A schematic diagram showing the 1×2 MZI with heater in one of the arms, (b) the 3-D simulation window showing the germanium waveguide and heater on a silicon substrate and (c) normalized spectra of the MZI before and after applying power.

temperatures above 90 K as,

$$\frac{dn}{dT} = 8.2443 \cdot 10^{-7} T + 0.00017234. \quad (1)$$

Since the optical confinement factor of the fundamental TM mode in the Ge waveguide core is 96%, only the thermo-optic effect in the Ge waveguide core is considered. To calculate the total phase shift introduced in the waveguide by dissipating a specific amount of power, we obtained the temperature profile as a line plot in the center of waveguide after which the local refractive index change was calculated using equation 1. The total experienced phase change was then calculated through numerical integration along the waveguide as

$$\Delta\phi = \int_0^L \frac{2\pi}{\lambda} \Delta n(z) dz \quad (2)$$

where λ is the wavelength of operation, $\Delta n(z)$ is the change in refractive index and L is the total length of the waveguide.

A typical measured transmission spectrum from the MZIs is shown in Fig.1(b). The insertion loss is 0.5 dB and the extinction ratio is -19 dB. The shift in destructive interference points is used to experimentally determine the obtained phase shift. The details on fabrication and measurement of Ge-on-Si PICs can be found in [7].

2. Ge-on-Si phase shifters

2.1. Standard phase shifter

We performed a Comsol simulation for the Ge-on-Si phase shifters as shown in Fig.2(a) and found that one requires 700 mW of power to achieve a 2π phase shift. The length of the heater was kept 700 μm and the corresponding temperature profile in the center of the waveguide along the length can be seen in Fig.2(b). This simulation was then confirmed by measuring the spectrum of the MZI as a function of applied power as shown in Fig.2(c).

We can immediately draw the conclusion that a heater designed in this configuration is very power inefficient. The main reason behind this is that the underlying silicon (thermal conductivity = 130 W/(m*K)) acts as a perfect heat sink which can also be seen in the simulation in Fig.2(a). An improvement in the design is thus needed to bring down the required tuning power. Since the majority of the heat is being sunk in the silicon substrate, a way to improve the efficiency of the thermo-optic phase shifter is by thermally isolating it from the silicon substrate.

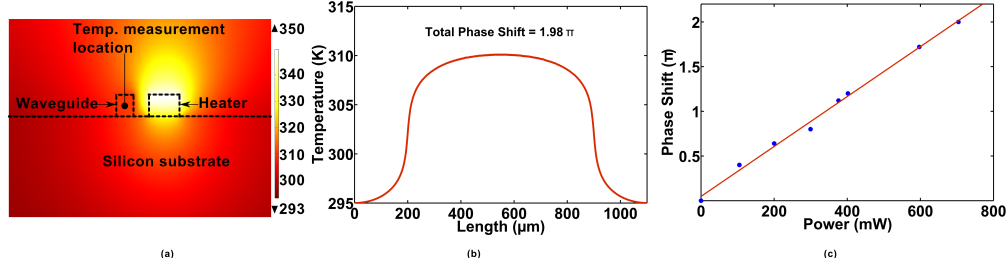


Fig. 2. (a) 2-D cross section in the middle of the simulation window, (b) line plot along the waveguide showing the temperature profile. The length of the heater was kept 700 μm and the power dissipated in the heater was 700 mW, (c) experimentally measured phase shift as a function of power dissipation along with the linear fit.

2.2. Fully undercut phase shifters

To prevent the heat to be sunk in the substrate, air trenches were created using a focused ion beam (FIB) tool on both sides of a heater/waveguide combination of length 210 μm as shown in Fig.3(a). The rest of the chip was protected by photoresist and lithography was performed to define the areas where FIB is to be done. While in this prototype FIB was used, this undercutting can be applied on a wafer scale through chemically assisted ion beam etching. The simulated 2-D cross section and the temperature profile along the waveguide can be seen in Fig.4(a) and (b) respectively. We confirmed the simulation results by measuring the phase shift as a function of applied power and found that 80 mW of power is required to achieve a 2π phase shift as seen in Fig.4(c).

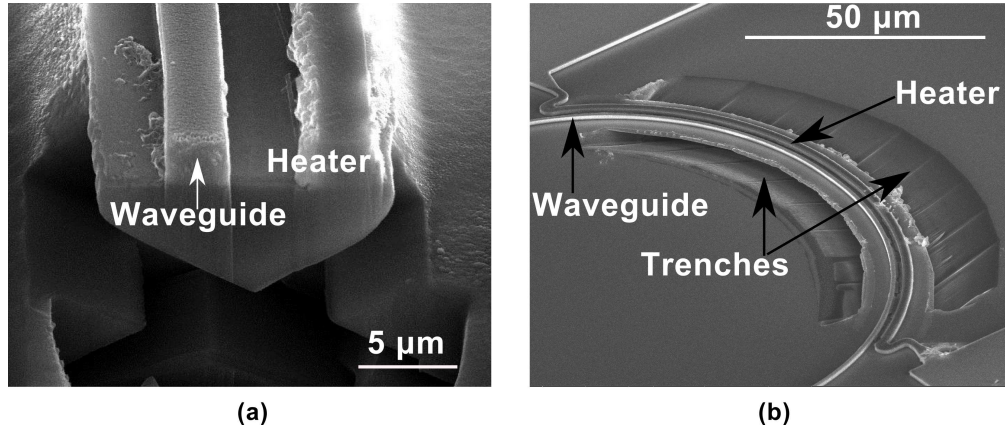


Fig. 3. (a) SEM image of fully undercut heater and (b) top view of a fully undercut heater.

3. Ge-on-SOI

As seen in previous section, isolating the heater from the conducting silicon substrate increases its efficiency. Although we have demonstrated a proof-of-principle concept using FIB, a more elegant way of solving this problem is to deliberately introduce a thermal insulator in the layer stack. Silicon dioxide (thermal conductivity = 1.4 W/(m*K)) can assist in confining the heat in the vicinity of the waveguide. Therefore we investigated Ge-on-Si-on-insulator as an alternative

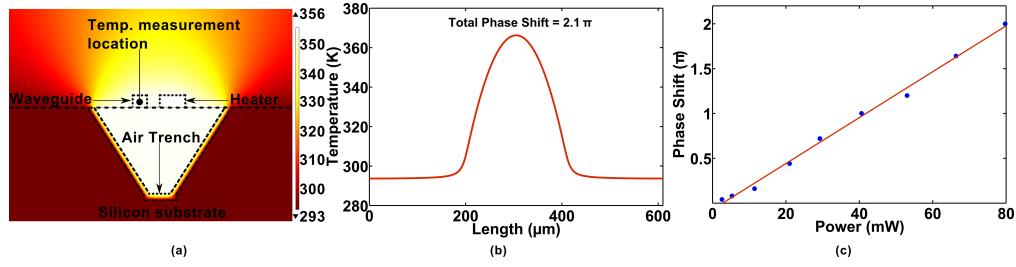


Fig. 4. (a) 2-D cross section in the middle of the simulation window of a fully undercut heater, (b) line plot along the waveguide showing the temperature profile. The length of the heater was kept $210 \mu\text{m}$ and the power dissipated was 80 mW . (c) experimentally measured phase shift as a function of power dissipation along with the linear fit.

waveguide platform for realizing efficient thermo-optic phase shifters.

SiO_2 however has a disadvantage in the mid-ir wavelength range since it strongly absorbs beyond $4 \mu\text{m}$ wavelength [12]. Therefore, it must be ensured that the light traveling in the Ge waveguide core is not affected by the buried oxide. The simulation of the loss of the fundamental TM mode at $5.3 \mu\text{m}$ as a function of the underlying Si layer thickness is shown in Fig.7(a) (assuming a $2 \mu\text{m}$ thick SiO_2). It can be seen that a Si thickness of $3 \mu\text{m}$ is sufficient to achieve low loss propagation.

The fabrication scheme of Ge-on-SOI phase shifters is described schematically in Fig.[5]. The process began with a 200 mm SOI wafer with 220 nm silicon thickness which received an

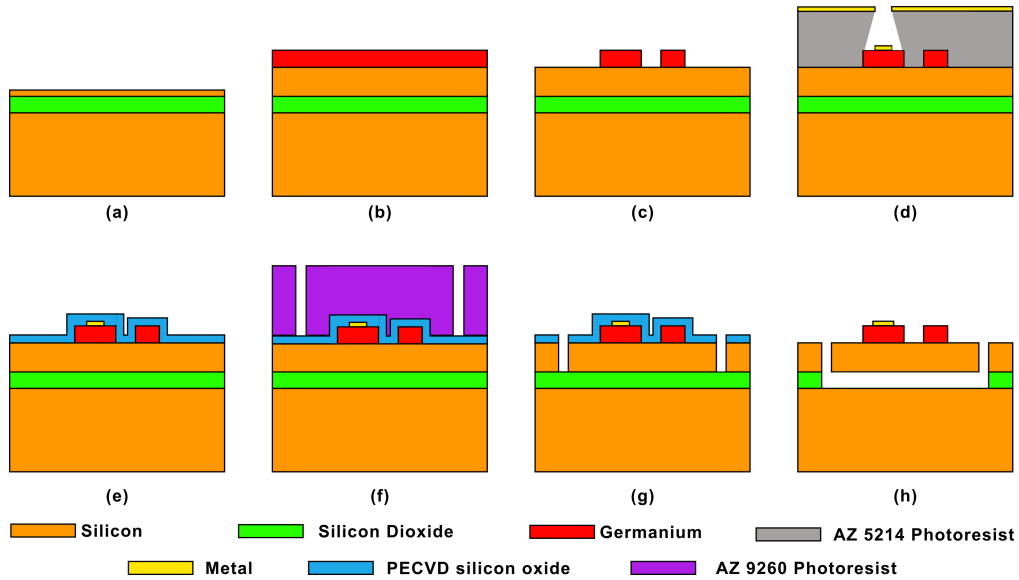


Fig. 5. Schematic fabrication scheme of Ge-on-SOI phase shifters (a) 200 mm SOI wafer with 220 nm silicon layer, (b) epitaxial growth of $3 \mu\text{m}$ thick silicon and $2 \mu\text{m}$ thick germanium layers, (c) waveguide definition by lift-off and dry etching, (d) lithography and metal deposition, (e) PECVD oxide deposition, (f) lithography for defining trenches, (g) dry etching of PECVD silicon oxide and silicon and (h) removal of PECVD oxide and buried oxide by HF dip

IMEC-clean [13]. 3 μm of silicon was then grown epitaxially in a horizontal, cold wall, load lock reactor (ASM Epsilon 2000). The in-situ bake at 1050°C removed all traces of oxygen. The silicon layer was grown at a temperature of 1050°C using dichlorosilane as silicon precursor and H_2 as carrier gas. The germanium layer was grown at 450°C using germane as precursor and H_2 as carrier gas. The wafer was then annealed at 800° C for three minutes to reduce the threading dislocation density. The germanium waveguide and heater were defined using a metal mask which was patterned using i-line lithography and lift-off. Germanium etching was carried out in a $\text{CF}_4:\text{O}_2$ plasma and the metal was removed by a HF dip. Metal lines on top of the germanium heaters were defined using a second lithography step and lift-off. Trenches were then defined in the silicon substrate using lithography and dry etching in $\text{SF}_6:\text{O}_2$ plasma. The samples were then thinned and cleaved. To achieve even better isolation samples were put in HF to remove the underlying SiO_2 . SEM images showing an undercut Ge-on-SOI heater section and the top view of such a heater incorporated in a MZI can be seen in Fig.6 (a) and (b) respectively.

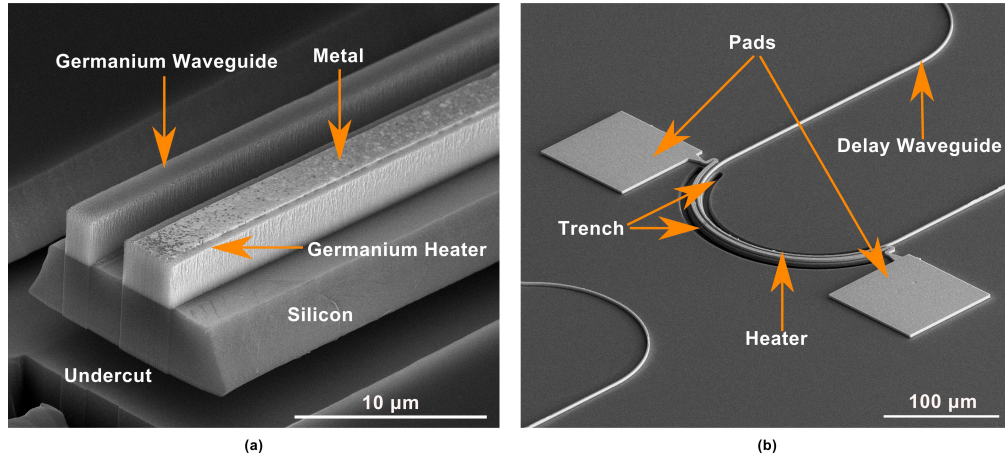


Fig. 6. SEM image showing (a) the cross section of the Ge-on-SOI waveguide where the underlying oxide has been removed and (b) top view of a MZI with a heater on one of the arms.

The waveguide loss of Ge-on-SOI single mode waveguides (2.2 μm wide) was found to be 7 dB/cm in the 5.25 - 5.35 μm wavelength range as can be seen in Fig.7(b). The origin of these higher losses compared to the values reported in Ge-on-Si [7] are not yet fully understood. Nevertheless such loss values are still sufficient to make mm-length scale integrated devices.

3.1. Ge-on-SOI phase shifters

To evaluate the performance of the Ge-on-SOI phase shifters, we performed previously described Comsol simulations the results of which are shown in Fig.[8](a) and Fig.[8](b). Since the undercut by FIB was done on a 210 μm long heater, we measured the phase shift as a function of dissipated heat on a heater of similar length as shown in Fig.[8](c) and found that the results match well with the simulations. The heater performance as a function of length was also studied using Comsol by calculating the tuning power required to achieve a phase shift of 2π and it was found that it decays rapidly at first becoming almost constant for longer heaters. This can be explained by the longitudinal flow of heat along the waveguide which at its end is connected to a large silicon slab acting as a good heat sink. This especially affects the shorter heaters since for longer devices the thermal resistance for the longitudinal heat flow becomes

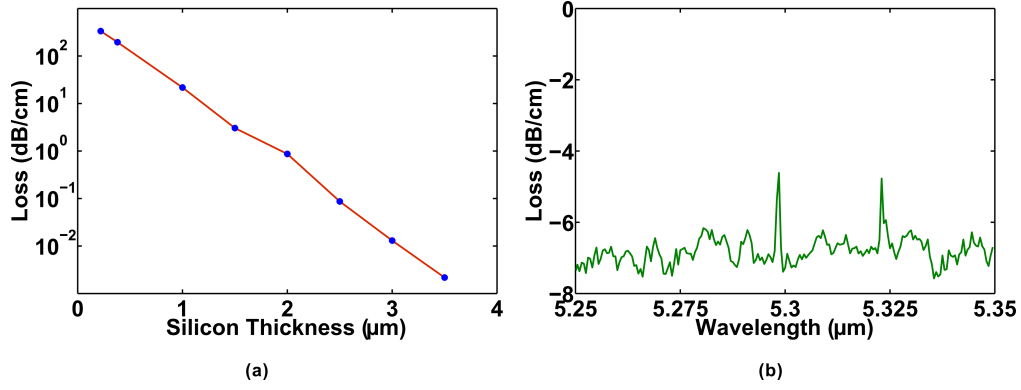


Fig. 7. (a) Simulation showing the absorption loss of the fundamental TM mode in the germanium-on-SOI waveguide as a function of silicon thickness and (b) measured waveguide loss.

larger. This was also verified experimentally the results from which are plotted together with the simulation results shown in Fig.[10](a).

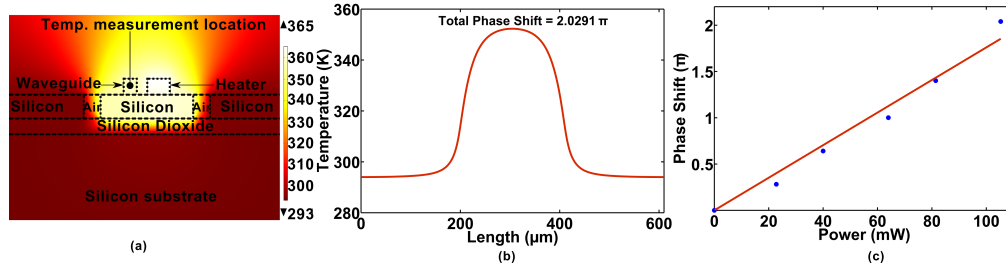


Fig. 8. (a) 2-D cross section in the middle of the simulation window of a Ge-on-SOI heater, (b) line plot along the waveguide showing the temperature profile. The length of the heater was kept 210 μm and the power dissipated was 100 mW. (c) experimentally measured phase shift as a function of power dissipation along with the linear fit.

3.2. Ge-on-SOI phase shifters with undercut

As described previously, the efficiency of the heater will increase if it is thermally isolated from the highly conducting silicon substrate. To enhance this, we removed the buried oxide using HF etching and carried out the measurements of the phase shift as a function of applied power for a heater of length 210 μm . It was found that a power of 20 mW is enough to achieve a 2π phase shift as seen in Fig.[9](c) which also agrees with the Comsol simulation as can be seen in Fig.[9](a) and (b). For heaters longer than 280 μm , it was observed that the free standing germanium waveguide and heater start bending and touch the substrate which results in a parasitic heat sinking path which hence again increases the required heating power. Taking into account this bending, the optimum configuration consists of a 280 μm long phase shifter, which dissipates 16 mW of power for a 2π phase shift. The simulation for tuning power required for a 2π phase shift as a function of length can be seen in Fig.[10](b) which indicates that the graph would follow a similar trend as described in previous section, if the free standing section would not bend and touch the silicon substrate.

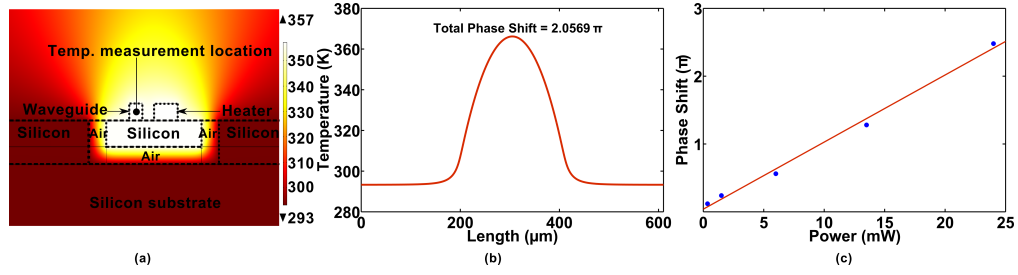


Fig. 9. (a) 2-D cross section in the middle of the simulation window for an undercut Ge-on-SOI phase shifter, (b) line plot along the waveguide showing the temperature profile. The length of the heater was kept 210 μm and the power dissipated was 20 mW. (c) experimentally measured phase shift as a function of power dissipation along with the linear fit.

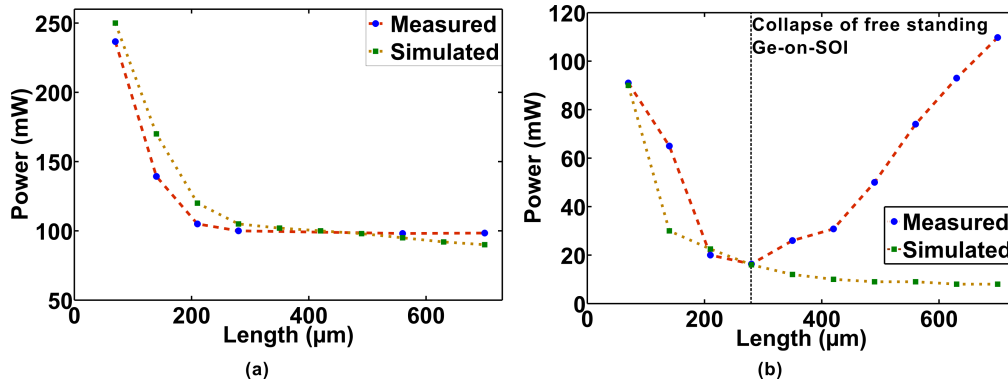


Fig. 10. Tuning power to achieve 2π phase shift as a function of length for a Ge-on-SOI phase shifter (a) without undercut and (b) with undercut.

4. Conclusion

In conclusion, we have demonstrated thermo-optic phase shifters for the mid-ir for the first time on the Ge-on-Si and Ge-on-SOI waveguide platform. Thermo-optic phase shifters in different configurations have been studied and a new waveguide platform (Ge-on-SOI) has been demonstrated which brings down the required tuning power from 700 mW to 16 mW. This paves the way to the power efficient tuning of mid-infrared photonic integrated circuits.

5. Acknowledgment

This work was supported by FP-7-ERC MIRACLE. Yosuke Shimura would like to thank FWO for a Pegasus scholarship.