PAPER

A Current-Steering DAC Architecture with Novel Switching Scheme for GPON Burst-Mode Laser Drivers

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SUMMARY This paper describes a current-steering Digital-to-Analog Converter (IDAC) architecture with a novel switching scheme, designed for GPON Burst Mode Laser Drivers (BMLD) and realized in a 0.35 μm SiGe BiCMOS technology with 3.3 V power supply. The (4+6) segmented architecture of the proposed 10-bit IDAC is optimized for minimum DNL (Differential Nonlinearity). It combines a 4-bit MSBs (Most Significant Bits) unit-element sub-DAC and a 6-bit LSBs (Least Significant Bits) binary-weighted sub-DAC. A switching scheme based on this dedicated architecture yields a high monotony and a fast settling time. The linearity errors caused by systematic influences and random variations are reduced by the 2-D double centroid symmetrical architecture. Experimental results show that the DNL is below ± 0.5 LSB and that the settling time after the output current mirror is below 12 ns. Although the proposed IDAC architecture was designed for a BMLD chip, the design concept is generic and can be applied for developing other monotonic high-speed current-mode DACs.

key words: current steering digital-to-analog converter, DNL, GPON, cascade current mirror, BiCMOS

1. Introduction

A traditional high speed laser driver has two differential pairs (Fig. 1), each powered by a current source, providing independently gated bias (I_{BIAS}) and modulation current (I_{MOD}). But for a low power supply (3.3 V) DC-coupled 1.25 Gbit/s laser driver with tail currents ranging from 1 to 80 mA, this architecture cannot achieve satisfactory performance. The major disadvantage of DC-coupling the driver to the laser diode (LD) is that the forward voltage drop of the laser diode (maximum 1.6 V) reduces the collector-emitter voltage (V_{CE}) swing of the output transistor. And the performance of the switching transistors depends heavily on V_{CE} and on the collector current I_{C} . The lower V_{CE} , the slower the transistor becomes, and the narrower the useful collector current range.

A DC-coupled 1.25 Gbit/s Burst Mode Laser Driver (BMLD), as specified in the ITU-T Recommendation G984.2 [1], has been designed as one of the key components of a Gigabit-capable Passive Optical Network (GPON) [2]–[4]. The 0.35 μm SiGe BiCMOS process was chosen to satisfy the primary requirements for a generic BMLD chip containing a substantial amount of digital circuitry. Simulations

Fig. 1 Traditional burst-mode laser driver stage.

Fig. 2 GPON burst-mode laser driver stage [3].

based on this technology at 3.3 V power supply showed that a single differential pair cannot be fast enough over a 1 to 80 mA collector current range.

For this reason, one differential pair was split in 8 branches having different tail currents in the burst-mode laser driver stage architecture [3] as shown in Fig. 2. Two such circuits are used to switch I_{BIAS} and I_{MOD} . The data path generates the inputs V_{INP} , V_{INN} based on the incoming data or the TH (Transmit High) signal. Thus low bias or modulation currents are supplied by a single differential pair, whereas the largest currents use 8 differential pairs in parallel.

To reach the specification of the BMLD under G984.2 and taking the laser driver stage structure [3] into account, a custom designed 10-bit current-steering Digital-to-Analog converter (IDAC) with a new switching scheme is proposed

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Fig. 3 10-bit IDAC architecture.

in this paper, which comprises 8 separate current outputs acting as 8 current sources. It is the switching scheme together with its related digital circuits that makes the IDAC having a good transient behavior as well as the monotonic performance. Two identical 10-bit IDACs are used to independently provide bias and modulation current between 1 and 80 mA with a high linearity and a short settling time. The IDACs are not interconnected directly with the differential pairs of the laser driver, because the output capacitance of the IDAC would reduce the output impedance at higher frequencies and deteriorate the current switching behavior of the laser driver. A cascade transistor could solve this problem but the extra voltage drop cannot be tolerated. So the IDAC currents are transferred to the differential pairs via current mirrors (Fig. 3) optimized for speed and power consumption, to not deteriorate the IDAC settling time.

2. Architecture with a Novel Switching Scheme

The architecture of the IDAC is shown in Fig. 3 and a switching scheme is proposed for fast settling and low glitch energy. Basically, it is a 10-bit segmented architecture that has been implemented with a 4-bit unit-element sub-DAC and a 6-bit binary-weighted sub-DAC. The segmented current-steering topology was chosen for a high monotony. To be compatible with the laser driver architecture [3] (Fig. 2), the IDAC must sink the current into 8 identical fast NPN current mirrors which build the IDAC output stage. The segmented current steering architecture of Fig. 3 shows 16 segment current sources (I_0 to I_{15}) and 6 weighted current sources. The currents are switched to

8 output current mirrors (Mirror 0 to Mirror 7) (to be discussed in Sect. 5) to be compatible with the laser driver architecture [3]. Eight unity-gain voltage buffers (to be discussed in Sect. 4) acting as the dummy mirrors which make the voltage at the negative current output of IDAC equal to the voltage at the positive current output. A small current ($5\mu\text{A}$) is added to the input of the output current mirrors as a pre-bias current which can increase the settling time of this mirror considerably.

I_{OUT0} to I_{OUT7} in Fig. 3 are the same currents as in Fig. 2, which represents the current amplified by a 1:12 current mirror. Every segment current from I_0 to I_{15} ($437.5\mu\text{A}$) is generated by a high-swing low-voltage cascade PMOS current mirror, made up of 64 unit current sources I_{unit} . Switching the 6-bit LSBs (Least Significant Bits) sub-DAC from segment current source to segment current source as in [5] would be better for the Differential Nonlinearity (DNL) but this makes the settling time longer, as the number of switches increases and the decoder becomes more complex. The 4 MSBs (Most Significant Bits) control 15 two-way switches of the 4-bit MSBs unit-element sub-DAC, switching between segment current sources I_1 to I_{15} and 8 output current mirrors; whereas the 6 LSBs control the 6 nine-way switches of the 6-bit LSBs binary-weighted sub-DAC. The 6-bit LSBs sub-DAC is always connected to current source I_0 , but with a flexibility to sink this segment current to all 8 output current mirrors by 6 independent nine-way switches inside the sub-DAC. Two diodes are cascaded between the negative output of the 6-bit LSB DAC and the ground in order to balance the voltages at the different outputs, and a voltage buffer as used between IDAC positive and negative

Table 1 IDAC switching scheme.

digital input codes	I_0 (LSB IDAC)	I_1	I_2	I_3	I_4 ... I_{13}	I_{14}	I_{15}
0000-XXXXXX (0~63)	M0	X	X	X	X	X	X
0001-XXXXXX (64~127)	M0	M0	X	X	X	X	X
0010-XXXXXX (128~191)	M1	M0	M0	X	X	X	X
0011-XXXXXX (192~255)	M1	M0	M0	M1	X	X	X
...	...	M0	M0	M1	...	X	X
1110-XXXXXX (896~959)	M7	M0	M0	M1	...	M6	X
1111-XXXXXX (960~1023)	M7	M0	M0	M1	...	M6	M7

current output is not possible in the 6-bit LSB DAC because these currents can be switched to 9 different outputs.

Table 1 shows the switching scheme where M0 ... M7 denotes Mirror 0 ... Mirror 7, and "X" indicates that the current source switches to its unused negative current output (I_{DUMMY}) without contribution to the positive current output (I_{OUT}). For example when the 4 MSBs are "0000" the 6-bit LSBs sub-DAC is connected to Mirror 0 while I_1 to I_{15} are connected to I_{DUMMY} . When the 4 MSBs are "0001" the 6-bit LSBs sub-DAC and I_1 are connected to Mirror 0 while I_2 to I_{15} are connected to I_{DUMMY} . When the 4 MSBs are "0010" the 6-bit LSBs sub-DAC is connected to Mirror 1, and I_1 and I_2 are connected to Mirror 0, while I_3 to I_{15} are connected to I_{DUMMY} .

The monotony can be shown in the following example: the transition from bit pattern 0001-111111 (127 in decimal) to 0010-000000 (128 in decimal) corresponds to

$$\begin{aligned}
 0001 - 111111 : I_{OUT} &= \left(\frac{63}{64} I_0 + I_1 \right) \times R_{M0} \\
 0010 - 000000 : I_{OUT} &= \frac{0}{64} I_0 R_{M1} + (I_1 + I_2) \times R_{M0} \quad (1)
 \end{aligned}$$

where R_{M0} (R_{M1}) is the ratio of Mirror 0 (1). If the matching of I_0 to I_{15} and the linearity of the 6-bit LSBs sub-DAC are appropriate, then the IDAC is monotonic. In this case the latter current is larger than the former one when I_0 to I_{15} are properly matched. So a 10-bit monotonic behavior is obtained independent of the mismatch of the ratios of the different current mirrors.

For transitions of the 6 LSBs the binary-weighted architecture can easily guarantee monotony by proper circuit design. The 6-bit LSBs sub-DAC generates the currents I_{UNIT} , $2I_{UNIT}$, $4I_{UNIT}$, $8I_{UNIT}$, $16I_{UNIT}$ and $32I_{UNIT}$. These six currents are each switched by a nine-way switch to one of the eight current mirrors or to its negative output. Every fraction has its own switch because this yields faster settling. Otherwise a series connection of a two-way switch

for every segment (from I_{OUT} to I_{DUMMY}) and an eight-way switch (from Mirror 0 to Mirror 7) would be needed, which results in slower settling due to the series connection of the switches. The advantage of this novel switching scheme is that a very fast settling time as well as a high monotony can be obtained by sacrificing absolute accuracy (due to mismatches of the R_M current mirror ratios). For this application, absolute accuracy is not required as the setting of the IDAC is controlled by an APC (Automatic Power Control) feedback loop [3], [6].

3. Design for Monotony

In a monotonic DAC, the analog output always increases as digital input increases. The DNL is the worst-case deviation from an ideal one-LSB step between two subsequent output codes. The INL (Integral Nonlinearity) is defined as the maximum deviation from a linear approximation to the DAC's real transfer function [7].

Due to the high-accuracy requirement of the power level monitoring circuitry, and its associated closed-loop digital APC algorithm [6], monotony is a very important design specification, especially during the calibration of the level monitoring, of the proposed IDAC besides design goals concerning speed and die area. In our application, DNL is much more important than the INL because a monotonic step of the accurate bias or modulation current with the digital input code has to be guaranteed for the reliable and accurate power level monitoring with the APC algorithm.

3.1 Current-Steering Architecture

For the design of high speed circuits in a recent semiconductor technology, the current-mode approach has distinct advantages over its voltage-mode counterpart. Many high-speed laser drivers have a current-steering architecture. Current-steering DACs are based on an array of matched current sources that are switched to the output. Three different basic architectures are possible depending on the implementation of this array, namely the unit-element, the binary-weighted, and the segmented architecture.

An IDAC with a unit-element architecture has a guaranteed monotonic behavior and a small DNL error since an additional, nearly identical unit current source is switched to the output for each LSB input increase in a thermometer-code approach. A major disadvantage of the unit-element architecture is its complexity, requiring the interconnection of a large number of current sources and switches. Although a binary-weighted implementation can take advantage of its inherent simplicity and the smaller area, it shows a much larger DNL error and dynamic error.

To get the best of both worlds, the two previous architectures are often combined into what is called a segmented architecture [8], [9], where an N -bit DAC is divided into two sub-DACs: M less significant bits are implemented in a binary-weighted architecture while the $(N-M)$ more significant bits are implemented in a unit-element architecture.

Fig. 4 Simplified block diagram of the 10-bit segmented IDAC.

The optimum balance among monotony, speed, silicon area and complexity can be found by selecting the value M correctly.

The formulas (2) and (3) define the DNL/INL and mathematically represent the idea behind the segmented architecture.

$$\text{DNL} \cong 2\sqrt{2^M} \left(\frac{\sigma_I}{I} \right) \text{LSB} \quad (2)$$

$$\text{INL} \cong 2\sqrt{2^{N-1}} \left(\frac{\sigma_I}{I} \right) \text{LSB} \quad (3)$$

Note that (σ_I) represents the standard deviation of the unit current sources, assuming a normal distribution for the unit current sources.

The selection of a $(4 + 6)$ segmented structure results from an optimum balance of DNL and speed performance, and is based on simulations. Figure 4 shows the simplified block diagram of the 10-bit segmented IDAC. It mainly consists of an 8×16 current sources matrix, a thermometer decoder, latch arrays and other associated digital circuitry. The pattern of the current sources matrix is designed for good matching, and will be described in detail in Sect. 6.

3.2 Sizing the Unit Current Source

In order to meet a DNL specification of 0.5 LSB with this $(4 + 6)$ segmented topology, a minimum requirement is that each and every unit current source of the IDAC has a current error smaller than 0.5 LSB . Herewith from formula (2), we can get:

$$\text{DNL} < 0.5 \text{ LSB} \Rightarrow \left(\frac{\sigma_I}{I} \right) < 3.125\% \quad (4)$$

Based on the established parameter mismatch statistical model [10], an expression can be derived for the gate-area $(WL)_{\min}$ of the unit current source transistor as a function of the gate voltage overdrive:

$$(WL)_{\min} = \frac{1}{2} \left[A_{\beta}^2 + \frac{4A_{VT}^2}{(V_{GS} - V_T)^2} \right] \left/ \left(\frac{\sigma_I}{I} \right)^2 \right. \quad (5)$$

W and L are channel width and length, A_{VT} and A_{β} are mismatch technology parameters, and $(V_{GS} - V_T)$ is the gate overdrive voltage of the current source PMOS transistor.

Using the simple square-law drain current model of a PMOS transistor,

$$\begin{aligned} \left(\frac{W}{L} \right)_{\min} &= I_D \left/ \left[\frac{KP_p}{2} (V_{GS} - V_T)^2 \right] \right. \\ &= \left[(I_{FS} / (2^N - 1)) \right] \left/ \left[\frac{KP_p}{2} (V_{GS} - V_T)^2 \right] \right. \end{aligned} \quad (6)$$

where KP_p is the transconductance parameter, and I_{FS} is the full-scale output current of the designed IDAC.

Regarding formula (4) and with two design constrains (formula (5) and (6)), the transistor size of the PMOS current cells can be defined. Based on this calculation, more accurate transistor dimensions can be acquired from Monte Carlo simulations.

4. Design for Speed

The upstream path of a PON operates in a multipoint-to-point TDMA (Time Division Multiple Access) scheme, where multiple ONUs (Optical Network Units) transmit upstream bursts towards a single OLT (Optical Line Terminator). So the BMLD in a given ONU must not send upstream light in timing windows allocated to other ONUs. And the BMLD transmit optical power level must be stabilized quickly within a short part of the time slots allocated to the specific ONU. To realize a fast initialization of the optical power by the APC algorithm, an IDAC settling time shorter than 12.8 ns is required, corresponding to 2 bytes at 1.25 Gbit/s . A distinction must be notified between the IDAC settling time and data bit rate since the latter is as fast as 800 ps (picosecond) guaranteed by the high-speed differential pair instead of the IDAC settling. Much faster transitions, of the order of 100 ps , are required to support an 800 ps bit width. This sub-nanosecond switching is realized by the high-speed differential pairs driving the laser, and by the optimized current mirror coupling between IDAC and differential pairs.

Although the current-mode approach can make the circuitry faster than its voltage-mode counterpart in a given technology, a traditional switching scheme of the segmented DAC [5], which normally has a series combination of switches on top of each other, is not qualified for our application. A novel dedicated switching scheme (described in Sect. 2) has been proposed in our design together with other circuitry improving the IDAC dynamic performance up to the design goal.

4.1 Latch, Two-Way Switch and Voltage Buffer

The dynamic performance of a current-steering DAC depends not only on the switching scheme but also on the properties of the latch and current switch. To minimize the settling time of the IDAC, a well-designed latch and two-way

Fig. 5 Latch and two-way switch with voltage buffer.

switch with a voltage buffer [11] is used. This low-power, 3.3 V BiCMOS voltage buffer is showing gigahertz operation, low output impedance and low input current. A super emitter follower is used to achieve low output impedance whereas base current compensation is used to reduce the input current.

The current is switched between 2 PMOS transistors, as controlled by the latch at the left side of Fig. 5. The major function of this latch is reducing the cross-point voltage of the differential control signals (Sel and the inverted Sel), in such a way that these transistors are never simultaneously in the off state. By doing so the voltage swing at the drain of the current source is reduced during switching. This swing must be limited because the current source has a considerable capacitance since the transistors are relatively big to achieve a good matching. We further reduced the settling time by using a unity-gain voltage buffer to make the voltage at the unused negative output of the IDAC (I_{OUTN}) equal to the voltage at the positive current output (I_{OUT}). This makes a considerable difference because I_{OUT} is fed into a current mirror of which the input voltage varies with the current. The unity-gain voltage buffer guarantees that the voltage at I_{OUTN} equals the voltage at I_{OUT} so that parasitic capacitances charge or discharge less when switching.

5. Description of Other Circuitry

5.1 Digital Part

The digital part is always an indispensable block of an IDAC, especially for a segmented architecture with a dedicated switching scheme, and includes decoding logic, synchronization logic, disabling and more. Figure 6 shows the digital function blocks of our 10-bit IDAC.

Since synchronization of digital control signals is far from ideal due to the routing and timing constraints tolerance, delay elements and retiming logic are necessary to reduce glitch energy and obtain fast settling. IDAC digital setting codes are generated by the APC algorithm in a 155 MHz clock domain ($1/8$ of 1.25 GHz). The value of the delay elements between the 155 MHz clock signal (Clk_155) and the digital code input (Bit<9:0>) was decided by accurate electrical corner simulations including temperature, power supply

Fig. 6 Digital part of the 10-bit segmented IDAC.

Fig. 7 (a) Segment current mirror and (b) output current mirror.

and process corners. This makes sure that all digital control signals from the decoder (SWA<15:1>, SWB<15:1>, B0<5:0>, ..., B5<5:0>) can be retimed by a clock edge at a correct moment to avoid digital hazards that could slow down the settling considerably.

To reduce power consumption, some parts of the BMLD circuitry can be disabled when no burst is sent upstream. This idle time is marked by an external, asynchronous transmit enable (TE) signal going low. The IDAC makes use of this asynchronous TE signal to reduce power consumption when no I_{BIAS} or I_{MOD} current is required. This is done by some simple combinatorial logic in the disabling block that makes the 10-bit input code 0 when TE = 0. A synchronizer built by two Flip-Flops avoids failures due to metastability.

5.2 Segment Current Mirror and Output Current Mirror

The segment current mirror of the 4 MSBs sub-DAC is shown in Fig. 7(a). It is actually a high-swing low-voltage PMOS cascade current mirror and the minimum voltage across the current sink is only $2(V_{GS} - V_T)$, which is one threshold voltage drop less than a regular cascade current mirror. The output resistance is still as high as for the regular cascade current mirror, which is very important for the

DNL performance of the IDAC.

The output 1:12 current mirror is shown in Fig. 7(b) [3]. This fast NPN current mirror amplifies the input current 12 times and may not deteriorate the settling time of I_{BIAS} or I_{MOD} . The mirrors operate for a low output voltage, as the V_{CE} of the differential pairs is about 400 mV. A mirror current gain of 12 was selected as a compromise between IDAC settling time and IDAC power consumption. Due to the high mirror output current, a considerable base current has to be driven. An NMOS follower delivers the base current, assuring a fast response at the cost of an extra current source (100 μA) in the follower. A gate-source capacitor is added for improving the high-frequency stability [12].

6. Double Centroid Symmetrical Layout

Current-mode DACs inherently suffer from static linearity errors due to systematic influences and random variations. Systematic mismatches originate from process biases, contact resistances, non-uniform current flow, temperature gradients, mechanical stresses and a host of other causes. Random mismatches come from microscopic fluctuations in dimensions, doping, silicon oxide thickness gradients and other parameters that influence component values [13].

The conceptual diagram of the 2-D double centroid symmetrical current sources matrix was shown in Fig. 4 and the layout of the realized 10-bit segmented IDAC is shown in Fig. 8. The 4-bit MSBs top-mirror current sources matrix contains the top group PMOS transistors of the cascade current mirrors of the 4-bit MSBs sub-IDAC.

To achieve good matching, a double centroid symmetrical architecture with identical unit transistors is selected. The 8×16 current sources matrix (Fig. 4) is made up of 4 centroid symmetrical quadrants and each of the quadrants is

a 4×8 centroid symmetrical matrix too. A double centroid architecture surrounded in a perimeter with dummy cells can minimize graded errors and compensate hierarchical errors. Every four unit-transistors are combined by local routing into a block-transistor in which most of inter-routing can be done inside the matrix, saving a considerable silicon area and layout effort.

The latches and the switches are placed in a separate array from the current sources. This is done to avoid coupling between the digital signals and the analog output signal. Another advantage of these separate arrays is that the layout area of a unity cell in the current source array can be minimized. In this way, the distances between the transistors are reduced, resulting in improved matching properties. Furthermore, digital coupling through the substrate has been reduced by the intensive use of substrate contacts and guard rings. To minimize the systematic error introduced by the voltage drop in the ground lines of the current-source transistors, sufficiently wide lines have been used. Special care has been taken to realize a symmetrical interconnection array in order not to degrade the matching performance. Throughout the whole design, layout parasitics have been taken into account. They have been manually extracted at each critical node and iterated in the electrical simulations. Good matching figures are obtained with a unit transistor of non-minimum size, compromising DNL, settling time and area.

7. Experimental Results

The proposed IDAC has been fabricated and successfully tested as one of the building blocks of a BMLD chip. The measurements have been made via the I_{BIAS} or the I_{MOD} output pin. Figure 9 shows the die micrograph. The die sized 4 by 4 mm is housed in a 68-pin VFQFPN package, and each 10-bit IDAC excluding output current mirrors has an active silicon area of 0.48 mm².

The IDAC monotony was measured at room temperature. The measurements were automated in a LabView platform communicating with the chip via SPI (Serial Pe-

Fig. 8 Layout of the realized 10-bit segmented IDAC.

Fig. 9 Die micrograph of BMLD chip.

Fig. 10 Measured DNL of the 10-bit IDAC.

Fig. 11 IDAC settling time at typical transitions, (a) from digital input code 0 to 255, (b) from digital input code 255 to 0.

ripheral Interface). The output voltage converted from the output current through a load resistor was measured with a high-resolution multi-meter. Figure 10 shows that the measured DNL falls between -0.260 LSB and $+0.166$ LSB. All tested IDACs showed a DNL below 0.5 LSB, proving that the DNL requirement is met.

The IDAC settling time is the amount of time it takes for the output current to settle to 90% of the input change. Figure 11 shows the measured transient curves at typical transitions from digital input code 0 to 255 in Fig. 11(a) and from digital input code 255 to 0 in Fig. 11(b). During these transitions, several two-way switches in 4-bit MSBs sub-DAC and all nine-way switches in 6-bit LSBs sub-DAC are switched between “ON” and “OFF” simultaneously. The fact that the settling time at these transitions is only a few nanoseconds proves that the proposed segmented IDAC with the novel switching scheme has a very fast transient behavior.

8. Conclusion

A fast and accurate 10-bit IDAC with segmented architecture was developed in a $0.35\text{ }\mu\text{m}$ SiGe BiCMOS process, and integrated into a GPON 1.25 Gbit/s BMLD chip. The segmentation shows 4 bits in the MSB section and 6 bits in the LSB section, which is the best trade-off between high monotony and fast settling time. A novel switching scheme is proposed compatible with the BMLD laser driver structure [3]. Experimental results confirm a DNL below 0.5 LSB and a settling time below 12 ns , which validates the effectiveness of the topology selection and the in-depth optimization of numerous circuit and layout, details.

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