A Silicon Backplane Technology for Microdisplays

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Abstract
In this paper a silicon backplane technology is described for the fabrication of high-resolution microdisplays. The technology is embedded in a 0.7 µm CMOS technology, and comprises DEMOS devices for enabling voltage spans of 12 V, and a special back-end processing module for planarizing the wafer and light shielding. This technology is used to develop a GXGA (2560x2048 pixels) microdisplay with 15 µm pixels on which the first results are reported.

1. Introduction
Recent reports on light-valve based display systems clearly show that liquid crystal on silicon is a promising technology for making reflective light valves. Several companies (JVC, IBM, Hitachi, Pioneer, ...) have reported successful results on these reflective microdisplay light valves. For front projectors, microdisplays will certainly be among the enabling technologies. However, also for rear projectors, with very large screen sizes and high resolutions, LC on silicon might become a serious alternative for CRT.

The first generation of microdisplays that resulted from our research on silicon backplane technology mainly aimed at personal viewer applications. Further refinement and research on DEMOS devices has resulted in the silicon backplane technology that is currently being used in the frame of the European Esprit research project MOSAREL[1]. Herein, the main objective is to build a GXGA projection light valve with 15 µm pixel size.

2. Silicon backplane
Our first successful result with LC on silicon was a 1/16 VGA prototype [2], which clearly proved the feasibility of this type of microdisplays. However, in order to cope with current and future needs, the specifications of this display were not sufficient.

Within the scope of MOSAREL, we further refined this technology. It has been mentioned [3] that for high-resolution backplanes, one should use a sub-micron CMOS technology, in our case the Alcatel Microelectronics 0.7 µm CMOS (C07). However, most standard sub-micron CMOS
can only handle a 5V voltage span. For deep sub-micron CMOS this is even 3.3V or less. In order to cope with the voltage requirements of the LC materials envisaged, the standard CMOS needed to be extended with a medium voltage process module capable of handling 12Vpp.

The n-type Drain Extended MOS transistor (n-DEMOS) was then used to make a custom layout of the pixel matrix, which is an analogue DRAM architecture (figure 1). The pixel pitch was chosen to be 15 µm.

2.1. DEMOS transistors

Two requirements played a major role in the development of the DEMOS devices. First, the size has to be limited, since the pixel pitch is only 15 µm. This is primarily of importance for the n-type pixel DEMOS. For the p-DEMOS, which is only used in the drivers, the pitch in one direction is also 15 µm, but in the other direction, the dimensions are much more relaxed.

Secondly, in order to keep the cost limited, C07 adjustments need to be minimal. This is especially true for the p-DEMOS. The n-DEMOS did not require any technological adaptations.

The results for the p-DEMOS, needed inside the drivers, have already been described in a previous paper [4]. For the pixel, a symmetrical n-type DEMOS was developed. Symmetrical, since the pixel transistor basically operates as a switch: both terminals must be floating. This can be seen from the schematic view in figure 1. Since the transistor is to be used as a switch, and \( V_{\text{bulk}} = V_{\text{substrate}} \), all voltages are referenced towards \( V_B = V_{\text{bulk}} \). With the aid of TCAD simulations, the influence of geometrical parameters on a series of working n-DEMOS transistors was studied (figure 2).

Figure 2. Drawing layout of n-DEMOS

The most important parameter in respect to the electric behaviour in the 0-15V region is the overlap of the n-well with the channel active area. Simulations predicted an increase of leakage current as the overlap \( O \) increases. However, another phenomenon occurs. Besides the gamma body effect on the threshold voltage, as with typical MOS devices, there is an anomalous body effect: a strong increase of \( V_{\text{th}} \) on top of the gamma effect. Both the \( V_{\text{source}} = -V_{\text{BS}} \) at which this effect starts to occur and the slope of the effect strongly depend on \( O \); as \( O \) increases they both decrease. With \( O > 0.5 \mu m \), the effect does not occur within the workable gate-range, as can be seen in figure 3. Both effects have been confirmed by experimental data.

Figure 3. Body effect variations with \( O \)

Whereas the leakage current is important for holding \( V_{\text{data}} \) on the storage capacitor, the body effect limits the maximum switchable \( V_{\text{data}} \) for a given maximum \( V_{\text{gate}} \). This implies a delicate choice of \( O \) for the pixel transistor. Since liquid crystal technologies are improving and a too elevated capacitor leakage results in poor or no image at all, \( O \) was chosen on the safe side regarding leakage. The first results of the MOSAREL backplane confirm the low
leakage (good image quality) and the high anomalous body effect (figure 4).

Figure 4. Measured data

From these in-matrix measurements, charging and discharging can be extrapolated. The most critical situation is the charging since in that case both electrodes’ voltages rise, inducing a high body effect, and thus reducing the current. For a storage capacitor of approximately 0.2pF and a gate-swing of 12V, Vdata can be up to 7 V as Traise,0.3% ~ 0.5 µs. (Tmax << 1/FrameRate,#rows = 1/100x2048 ~ 5µs)

2.2. AM: pixel-architecture

The next step was to incorporate the n-DEMONS into a pixel layout with a 15 µm by 15 µm pitch. One n-DEMONS is 17 µm long and 7 µm wide, including the required spacings to avoid a deep punch-through channel. This means that although small, it does not fit into a pixel. However, by taking one common drain for two adjacent pixels of the same column, the total length becomes 28.5 µm. This leaves some space to add a substrate contact to collect eventual harmful substrate currents. In order to enlarge the capacitor area, two transistor pairs are put aside, counting up to a width of 14 µm. The remaining 16 µm of this 2*2 pixel block is used for the four storage capacitors. This 2*2 block is then mirrored to further maximise the capacitor area. The capacitors are arranged in such a way as to minimise and equalise the capacitive coupling between the storage capacitor and the metal interconnect.

This 15 µm design for a GXGA display backplane results is a light valve with an active area of 38.4 mm x 30.7 mm. This does not fit in the field size of the I-line stepper used at Alcatel Microelectronics. This was solved by developing a stitching stepper job. Experimental results showed no visible artefacts in the active matrix along the stitching borders.

2.3. AM: back-end processing

Apart from the planarizing purpose of the back-end processing, in order to obtain highly reflective mirrors, the DRAM architecture also demands the back-end processing to provide a proper light shielding. Several schemes have been described in literature [5]. In our case we chose to add a deep sub-micron like metal back-end processing. This involves CMP, which is normally not included in C07.

The light blocking and absorption is obtained by forcing the light to undergo multiple reflections before possibly reaching the silicon. The multiple reflections are needed, since the lithographic antireflective layer (TiN) on top of the Al interconnect layers only poorly absorbs light in the visual region (e.g. 20% reflected green light for TiN with the appropriate thickness).

![Figure 6. Metal labyrinth light shield](image)

As seen in figure 6, the layout of the third metal is such that, in combination with the top Al pixel electrodes, light is reflected and absorbed sufficiently. Under an illumination intensity of 1.5 10^6 Lux the assembled backplane still operated well.

Figure 7. One top Al mirror electrode
Figure 7 shows a SEM picture of one electrode, illustrating the planarization. Clearly, only the metal3-metal4 via remains visible. The aperture ratio is 90.8% and the Al reflectance was measured at 88% which results in an overall reflectance of ~80%.

3. Liquid crystal technology

One of the LC-effects we use in this GXGA test-display is the Vertical Aligned Nematic LC effect (VAN-LC). The black as well as the white state are excellent. Randomly dispersed spacers were barely visible in the white state and virtually invisible in the black state. The filled assembly clearly showed that a silicon backplane technology is a feasible approach for very high-resolution microdisplays.

4. Conclusion

In this paper we showed the viability of using a silicon backplane for making very high resolution reflective microdisplays. DEMOS devices are incorporated and used with little changes to the standard CMOS. The light sensitivity of the silicon is adequately handled with an improved deep sub-micron back-end processing scheme and the first tests under high illumination show proper overall functioning of the GXGA test-display.