InP-based Membrane Photodetectors for Optical Interconnects to Si

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***Abstract*—We present the design, fabrication and acharacterization of an InP-based membrane photodetector on an SOI wafer containing a Si-wiring photonic circuit. Waveguide losses in the Si-wiring circuit are below 5 dB/cm. Measured detector responsivity is 0.45 A/W. The photonic device fabrication is compatible with wafer scale processing steps, guaranteeing compatibility towards future generation electronic IC processing.**

***Index Terms*—Optical Interconnects, InGaAs/InP, Photodetector, PICMOS.**

I. Introduction

FOR future generation electronic ICs, a bottleneck is expected at the interconnect level. The integration of optical sources, waveguides and detectors forming a photonic interconnect layer on top of the CMOS circuitry is a promising solution, providing bandwidth increase, immunity to EM noise and reduction in power consumption [1], [2], [3]. This solution is investigated within the European project PICMOS[1]. In that context, the interconnect layer is built as a passive Si photonic waveguide layer and the InP-based photonic sources and detectors are fabricated in a way compatible with wafer scale processing steps. This approach combines the advantages of high quality Si wires with the excellent properties of InP-based components for light generation and detection. The integration technique that is investigated here assures compatibility towards future generation electronic ICs and is based on a die-to-wafer bonding technology [4]. Experimental results on a full optical link, including lasers and detectors, were reported in [5]. In this paper, we will focus on the detector design, fabrication and characterization.

II. Design

In order to detect the light, it first has to be coupled from the Si wire into the detector structure. In our approach, that is realized by means of an InP membrane input waveguide on top of the SOI wafer containing the Si photonic wiring, like shown schematically in Fig. 1. The two waveguides act as a synchronous coupler that couples the light from the Si wire into the transparent InP waveguide that guides it to the absorbing detector region, which is on top of the transparent layer. The PD structure is built as an n.i.d. 700 nm InGaAs absorption layer sandwiched between a highly p-doped 50 nm InGaAs contact layer and a highly n-doped 250 nm InP layer, which is also used for realizing the membrane waveguide, and has a footprint of $5 \times 10\ \mu m^2$. We chose a total detector thickness of 1 μm in order to ease integration with the μ-disk lasers described in [6]. The thickness also results from a trade-off between device speed and efficiency. Due to the type of PD illumination, the most limiting factor for the speed is the carrier transit time in the diode depletion region. The detector predicted RC time and transit time constants are $\tau_{RC} = 4$ ps and $\tau_{tr} = 40$ ps, respectively, which leads to an expected 3-dB bandwidth of around 25 GHz [7]. Concerning the internal quantum efficiency, simulations show that more than 90% of the optical power is absorbed within 7 μm, as can be seen in Fig. 2. However, part of the power is absorbed in the p-doped contact layer and in the metal contact layer. The light absorbed in this region is lost, as it does not contribute to the generated photocurrent. Taking this into account, we conservatively predicted an internal quantum efficiency of

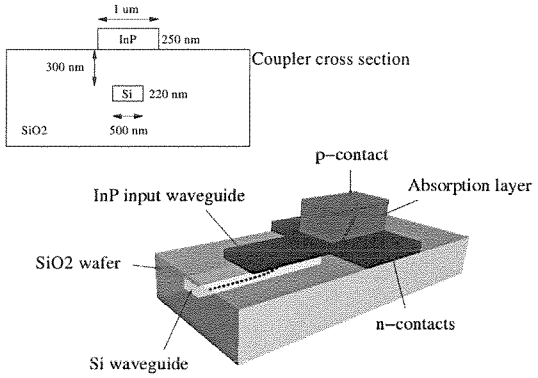

Fig. 1. Photodetector structure. The coupling from the Si photonic waveguide layer to the PD is realized by means of the InP membrane input waveguide, on top of which the detector is stacked. A cross section of the coupler is schematically shown.

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[1]Photonic Interconnect Layer on CMOS by Wafer-Scale Integration (PICMOS), http://picmos.intec.ugent.be

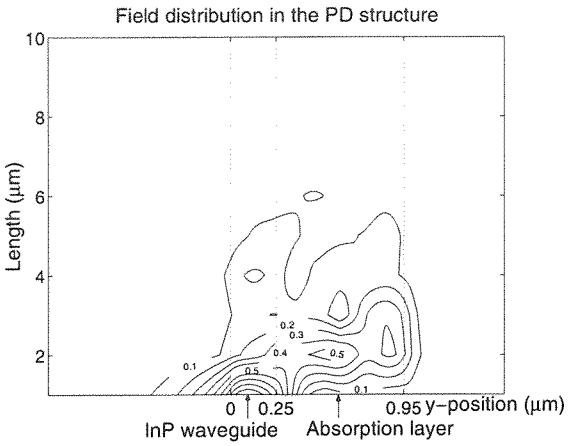

Fig. 2. The simulated field distribution in the photodetector after the interface between the input waveguide and the p-i-n strcture is plotted. Light propagating in the InP waveguide is coupled into the depletion layer of the PD. More than 90% of the power is absorbed within 7 μm.

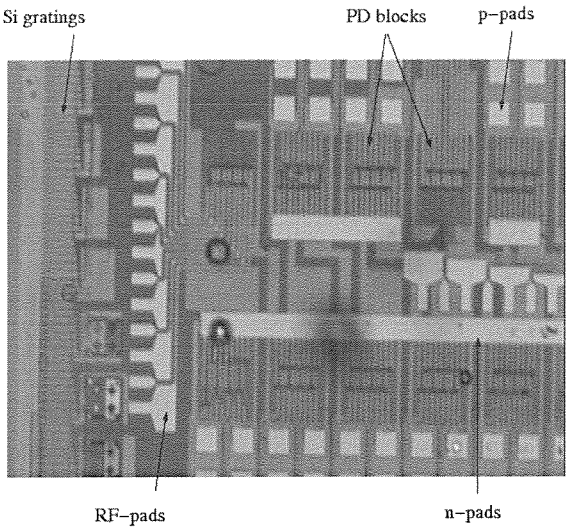

Fig. 3. Picture of the fabricated chip. Ten PD blocks (8 devices/block) are shown in this picture. DC and RF p- and n-contact pads are also visible, as well as the Si grating couplers (on the very left).

approximately 70%.

The detector input InP coupler was designed to achieve mode matching with the Si photonic waveguide, which is 500 nm wide and 220 nm thick (see Fig. 1). We fixed the InP waveguide thickness to 250 nm, which leads to a predicted optimum waveguide width of around 1 μm, calculated with two different full vectorial mode solvers. According to the simulations, the predicted coupling length is around 14μm, and a coupling efficiency of more than 80% can be achieved with a tolerance of $\pm$150 nm for the InP waveguide width, which is well within the current technology limitations. For more details about the InP membrane coupler design, we refer to our previous work described in [8]. The PD structure shown in Fig. 1 allows the fabrication of laterally tapered membrane waveguides, which provide an increase of the alignment tolerance between the waveguides without additional processing steps. Details about design and fabrication of the Si photonic waveguides are extensively presented in [9].

III. Fabrication

The PD layer stack described in the previous section was grown on a 2" InP wafer. It was sawn in dies that were then bonded upside down on an SOI wafer, in which the Si waveguide pattern had been defined, and the InP substrate was wet-chemically removed from the dies. The bonding technique used in the project consists in depositing a 200 nm thick layer of SiO_2 on top of the Si waveguides and a 100 nm thick SiO_2 layer on top of the InP wafer. When flipping the photonic dies upside down, the van der Waals molecular bonding forces at the SiO_2-to-SiO_2 layer interface provide die-to-wafer adhesion. We refer to [4] for more details about this technique. Afterwards, the PD pattern was defined by e-beam lithography and transferred to a 150 nm thick SiO_2 hard mask and the SOI wafer was sawn into samples hosting one photonic die each. The hard mask was then used to dry-etch the membrane waveguides and the PD bottom contact areas, which share the same n-InP layer. Then, the PD mesas were wet-chemically etched and a polyimide layer was deposited to planarize the chip surface and provide electrical isolation. Finally, top- and side-contact windows were opened by O_2 plasma-etch and RIE, respectively, and a Ti/Pt/Au metal layer stack was evaporated and patterned by lift-off. Grating fiber couplers were also integrated in the Si photonic waveguide layer to allow characterization of detectors without the need of a full optical link fabrication. Such gratings can be seen in the left part of Fig. 3 and are described more in detail in [10]. Fig. 3 shows a picture of the fabricated devices.

IV. Measurement Results

The device characterization was performed by using a tunable laser source to illuminate the detector and a Keithley source-meter unit to reversely bias the PD and to read out the generated photocurrent. First, the detector dark current at different applied bias voltages was measured. Results are shown in Fig. 4, which shows the diode I-V characteristic in reverse and forward bias working regimes. Dark currents around 1.6 nA were registered at -4 V.

A tunable laser source (TLS) and a polarization controller were used to couple TE-polarized light through the grating coupler into the Si waveguide. The photodiode generated photocurrent as a function of the applied bias voltage was measured for the following TLS output powers: 0 mW, 0.2 mW and 0.4 mW. To evaluate the detector efficiency, the following factors were considered. Firstly, the fiber connections from the laser source to the polarization controller and to the coupling input fiber cause a loss of 0.7 dB. Secondly, the Si grating coupler is wavelength dependent and has 20% optimum coupling efficiency at $\lambda = 1575$ nm. Lastly, Si waveguide

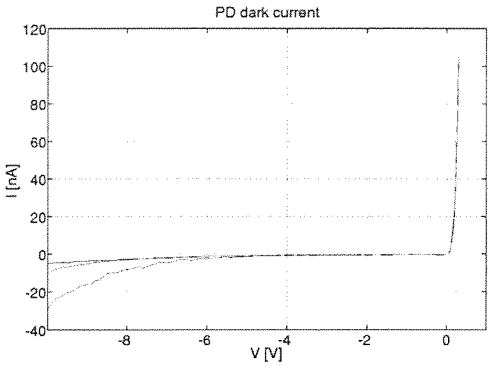

Fig. 4. Diode I-V characteristic in reverse and forward bias working regimes measured in the darkness. Dark current values around 1.6 nA were registered at -4 V.

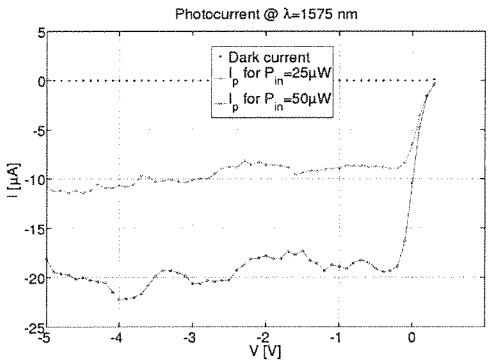

Fig. 5. Measured photocurrent for 0 μW, 25 μW and 50 μW optical input power as a function of the detector applied bias voltage.

measured losses are 4-5 dB/cm, for TE-polarized light [11]. That leads to a loss of 1.3 dB along the Si waveguide length of 3.2 mm, from the grating coupler to the detector input. Taking those loss sources into account, the detector optical input powers corresponding to the TLS intensities mentioned above are 0 μW, 25 μW and 50 μW. The responsivity of the PD structure was thus calculated to be $R = 0.45$ A/W, which is a conservative value, as the grating coupler maximum efficiency was assumed. Such responsivity corresponds to a quantum efficiency $\eta = 35\%$, which includes the efficiency of the InP membrane coupler and the internal quantum efficiency of the pin-detector itself. Measurement results are shown in Fig. 5, which also demonstrates the linear behaviour of the PD response to the incoming input power.

V. Conclusion

We presented an InP-based photodetector fabricated on a bonded SOI wafer containing Si waveguides, suitable for an optical interconnect layer on top of CMOS ICs. The PD footprint is 5×10 μm^2 and an InP membrane input waveguide is used to couple the optical signal out of the interconnect layer. Measurements recorded a detector responsivity R=0.45 A/W. That corresponds to a quantum efficiency η=35%, which includes the efficiency of the InP membrane input coupler and the internal quantum efficiency of the pin-detector itself.

Acknowledgment

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References

[1] *International Technology Roadmap for Semiconductors (ITRS)*, http://public.itrs.net.

[2] C. Piguet, J. Gautier, C. Heer, I. O'Connor, and U. Schlichtmann, "Extremely low-power logic," in *Proc.of the Design, Automation and Test in Europe Conference and Exhibition (DATE'04)*, vol. 1, Feb. 16-20 2004, pp. 656–661.

[3] D.A.B. Miller, "Optical interconnects to Si," *IEEE J. Sel. Topics in Quantum Electron.*, vol. 6, no. 6, pp. 1312–1317, Nov./Dec. 2000.

[4] L. Di Cioccio et al., "Recent results on advanced molecular wafer bonding technology for 3D integration on silicon," in *Wafer Bonding Conference*. Quebec, 2005.

[5] P.R.A. Binetti, J. Van Campenhout, X.J.M. Leijtens, M. Nikoufard, T. de Vries, Y. Oei, L. Di Cioccio, J.-M. Fedeli, C. Lagahe, R. Orobtchouk, X. Letartre, P. Regreny, P. Rojo-Romeo, C. Seassal, P.J. van Veldhoven, R. Notzel, D. Van Thourhout, R. Baets, and M.K. Smit, "An optical interconnect layer on silicon," in *Proc. 13th Eur. Conf. on Int. Opt. (ECIO '07)*. Copenhagen, Denmark, April 25–27 2007, post-deadline paper.

[6] J. Van Campenhout, P. Rojo Romeo, D. Van Thourhout, C. Seassal, P. Regreny, L. Di Cioccio, J.-M. Fedeli, C. Lagahe, and R. Baets, "Electrically pumped inp-based microdisk lasers integrated with a nanophotonic silicon-on-insulator waveguide circuit," *Optics Express*, vol. 15, no. 11, pp. 6744–6749, May 2007.

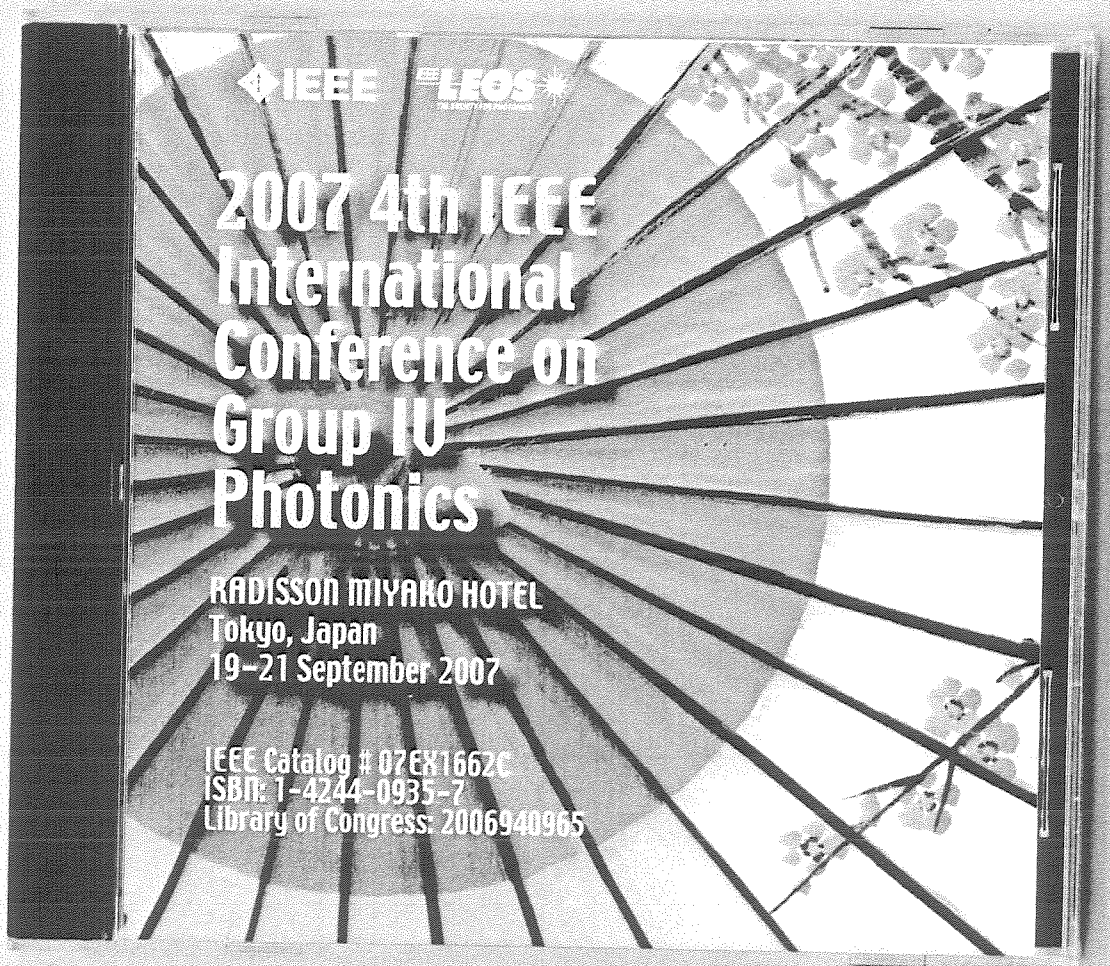
[7] P. Binetti, X. Leijtens, M. Nikoufard, R. Orobtchouk, T. Benyattou, T. de Vries, Y. Oei, and M. Smit, "A compact detector for use in photonic interconnections on CMOS ICs," in *Proc. IEEE/LEOS Symposium (Benelux Chapter)*. Mons, Belgium, Dec. 2005, pp. 233–236.

[8] P. Binetti, X. Leijtens, M. Nikoufard, T. de Vries, Y. Oei, L. Di Cioccio, J.-M. Fedeli, C. Lagahe, R. Orobtchouk, C. Seassal, P. van Veldhoven, R. Nötzel, and M. Smit, "Membrane couplers and photodetectors for optical interconnections on CMOS ICs," in *Proc. IEEE/LEOS Symposium (Benelux Chapter)*. Eindhoven, The Netherlands, 2006, pp. 237–240.

[9] D. Van Thourhout, P. Dumon, W. Bogaerts, G. Roelkens, D. Taillaert, G. Priem, and R. Baets, "Recent progress in SOI nanophotonics waveguides," in *Proc. 31st Eur. Conf. on Opt. Comm. (ECOC '05)*. Glasgow, Scotland, Sep. 25–29 2005, pp. 241–244.

[10] D. Taillaert, W. Bogaerts, P. Bienstman, T. Krauss, P. V. Daele, I. Moerman, S. Verstuyft, K. D. Mesel, and R. Baets, "An out-of-plane grating coupler for efficient butt-coupling between compact planar waveguides and single-mode fibers," *IEEE J. Quantum Electron.*, vol. 38, no. 7, pp. 949–955, Jul. 2002.

[11] B. Han, R. Orobtchouck, T. Benyattou, P. Binetti, S. Jeannot, J.-M. Fedeli, and X. Leijtens, "Comparison of optical passive integrated devices based on three materials for optical clock distribution," in *Proc. 13th Eur. Conf. on Int. Opt. (ECIO '07)*. Copenhagen, Denmark, April 25–27 2007, p. ThF3.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