8e UGent - FirW
DOCTORAATSSYMPOSIUM

woensdag 5 december 2007 | 14h00 | Het Pand | Onderbergen 1 | 9000 Gent

UNIVERSITEIT GENT

FACULTEIT INGENIEURSWETENSCHAPPEN

109

Hardware Accelerated Network Processors

Pieter Demuytere and Xing-Zhi Qiu
Supervisor(s): Jan Vandewege

As the bandwidth in computer networks is increasing more and more, network equipment struggles to process the millions of packets per second in a deterministic manner. We present a heterogenic setup of both a processor and dedicated hardware tackling this throughput issue. Using a mixed setup, the microprocessor can leave the high rate data plane processing to the dedicated hardware while handling the complex management itself. This split-up clearly has its advantages, but also comes with some drawbacks such as the limited interface between the two parts. The data plane processing block consists of C-programmable cores and dedicated hardware blocks. By combining pipelining and parallelism, a scalable and flexible data plane architecture is developed. Implemented in FPGA, the architecture can handle a throughput of at least 20 million Ethernet packets per second.

110

An Analytical Model for Superscalar Out-of-Order Processors

Stijn Eyerman and Lieven Eeckhout
Supervisor(s): Koen De Bosschere

Software simulations can estimate the performance of a newly designed, but not yet built, processor. They can be used to optimize the new processor's performance in a very early design stage. But simulations are extremely slow and are not useful for exploring large design spaces and multiple workloads. They also output raw numbers that don't provide enough insight into the processor's performance for the designer. Therefore we developed an analytical processor performance model, that not only predicts performance much faster than simulation, but also gives insight into how different events impact processor performance, and what the most efficient sizes are for different processor components. Starting from a fast analysis of the workload that has to be executed on the processor, we use interval analysis to predict performance and provide useful insights. The model can also be included in the hardware, to produce accurate performance characteristics for compiler and software builders.