113Gb/s (10 x 11.3Gb/s) ultra-low power EAM driver array

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Abstract: This paper presents an ultra-low power SiGe BiCMOS IC for driving a 10 channel electro-absorption modulator (EAM) array at 113Gb/s for wavelength division multiplexing passive optical network (WDM-PON) applications. With an output swing of $2.5V_{pp}$, the EAM driver array consumes only 2.2W or 220mW per channel, 50% below the state of the art. Both the output swing and bias are configurable between 1.5-3.0V_{pp} and 0.75-2.15V respectively.

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References and links

1. P. D. Townsend, A. Clarke, P. Ossieur, D. Smith, A. Borghesani, D. Moodie, I. Lealman, X.-Z. Qiu, J. Bauwelinck, X. Yin, K. Grobe, B. T. Teipen, R. Jensen, N. Parsons, and E. Kehayas, "Towards Colourless Coolerless Components for Low Power Optical Networks," *37th European Conference and Exhibition on Optical Communication (ECOC, Geneva, 2011)*, Tu.5.LeSaleve.
 2. E. Sackinger, *Broadband Circuits for Optical Fiber Communication* (John Wiley & Sons, Hoboken, 2005), Chap. 8.
 3. T. Yamase, M. Sato, H. Uchida, H. Noguchi, K. Sato, and T. Kato, "10-Gb/s In-line Centipede Electrode InP MZM and Low-Power CMOS Driver with Quasi-Traveling Wave Generation," in *Proceedings Optoelectronics and Communications Conference (OECC, 2011)*, pp. 61-62.
 4. A. Konczykowska, F. Jorge, C. Kazmierski, F. Blache, and J. Godin, "EAM DFF-Driver Optimization For 40 Gb/s Transmitter," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 12–17, 2005, pp. 1853–1856.
 5. D.-U. Li, L.-R. Huang, and C.-M. Tsai, "Low Power Consumption 10 Gb/s SiGe Modulator Drivers with 9 V_{pp} Differential Output Swing Using Intrinsic Collector-Base Capacitance Feedback Network," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC, 2005)*, pp. 317-320.
 6. S. Galal and B. Razavi, "10-Gb/s Limiting Amplifier and Laser/Modulator Driver in 0.18 μ m CMOS Technology," *IEEE J. Solid-State Circuits* **38**, 2138 – 2146 (2003).
 7. B. Liang, D. Chen, B. Wang, G. Situ, T. Kwasniewski, and W. Zhigong, "A Monolithic High Modulation Efficiency CMOS Laser Diode/Modulator Driver," in *International Conference on Telecommunications (ICT, 2009)*, pp. 361-363.
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1. Introduction

WDM technologies have been successfully deployed for many years in metro and core networks; they provide tremendous system capacity with long distance transmission. Lately, service providers are deploying passive WDM technologies for wireless/wireline backhauling, business connectivity, and fiber-to-the building (FTTB) applications. In access networks, however, WDM technology is not commonly used yet. This is due to the relatively low required per-user data rates at present and more importantly due to the higher cost needed to deploy entire WDM access networks compared to already massively deployed time division multiplexing (TDM) PONs. There is a strong need for new WDM access components which are compact, cost-competitive and mass-manufacturable, in particular at the optical line termination (OLT) of a central office (CO) where high degree integration is a must. While a WDM-PON OLT could in principle be built from pluggable transceivers, a cost-, footprint- and energy-optimized solution is not available today, mainly due to the lack of highly integrated multi-channel transceiver arrays [1].

A reflective WDM-PON network as shown in Fig. 1 was proposed in [1]. The major component integration challenge for this scheme is at the OLT. In its downstream direction 10 wavelength channels of reflective transmitters (R-TXs) using 10 reflective electro-absorption modulators (REAMs) are integrated into an array. One of the most challenging components to be developed for R-EAM TXs is an ultra-low power consumption 10 channel EAM/REAM driver array operating at 10-11.3 Gb/s data rates. As typically a discrete EAM driver consumes 1W, integrating 10 such EAM devices into a single array would require a total power consumption of 10W, which is much too high for a single IC to handle without a costly, power consuming thermo electric cooler (TEC). By lowering the power consumption of the drivers, TECs can be avoided, giving components that aren't only compact and cost-efficient, but also energy-efficient.

Fig. 1. Reflective WDM-PON network

In this paper, an array of 10 EAM drivers at 10-11.3Gb/s each is presented, to achieve a total data rate of 113Gb/s. To the best of our knowledge such EAM driver arrays are not currently available on the open market, nor published in the literature. This is the first 10 channel driver array for EAMs and the lowest power consumption for an EAM driver so far reported, 50% below the state of the art.

The remainder of this paper is organized as follows. The next section illustrates the chip

level architecture of the EAM driver array. Different techniques to reduce the power consumption are explained in section 3. The fourth section presents the experimental results. After that the power consumption of the designed array is discussed and compared to the state of the art in section 5. Finally, conclusions are drawn in the last section.

Fig. 2. EAM driver array IC building blocks with DC-coupled outputs.

2. EAM driver chip architecture

Figure 2 depicts the simplified building blocks of the EAM driver. It includes an input that is differentially matched to 100Ω , a predriver block to amplify the input signal and to drive the large capacitive input of the driver output stage. This predriver can also control the pulse width to compensate for the non-linearity of the (R)EAM. The predriver is directly followed by an EAM driver stage, which can control the bias current and modulation current of the EAM modulator. The control is implemented using a serial peripheral interface (SPI), which can set both the bias and modulation current with a 4-bit resolution. The bias and modulation current can be set independently for every channel to optimize the settings of the 10 EAMs according to the transmitted wavelength.

3. Power consumption reduction techniques

Figure 3(a) shows a simplified schematic of the driver output stage in order to clarify the origins of the driver power consumption [2]. Keeping in mind that the EAM needs a swing between 2 and $3V_{pp}$, one can identify a number of reasons for the large power consumption of commercial drivers, which is typically as high as $1W$ for a single driver. First of all, there is a necessity for a high supply voltage to provide sufficient headroom for transistors when generating the required relatively large output swings. For commercial EAM driver ICs, $5.2V$ is a recurring supply voltage (V_{cc2} in Fig. 3(a)), which is used for all building blocks in the IC. However, most blocks can operate at much lower power supplies. Secondly, the EAM is typically shunted by a 50Ω termination resistor and as the EAM and driver are several inches/cm apart in most cases, the output impedance of the driver IC also needs to be 50Ω , to minimize reflections. As a consequence, the driven load is 25Ω , which means an output swing of $2.5V_{pp}$ requires a modulation current, I_{MOD} , of $100mA$. This yields a power consumption of $520mW$ in the last stage alone, when the supply is $5.2V$. In third place, the driver stage uses a differential pair, while only a single-ended output is needed for the EAM. The pair switches the modulation current between the right arm, containing the EAM, and the left arm,

connected to a dummy load to preserve symmetry. Since only the right arm drives the EAM, the current in the left arm is a waste of power

Fig. 3. Simplified driver output stages, (a) typical, (b) reduced power.

These observations led to a new design, combining different power reduction techniques as shown in Fig. 3(b). Unfortunately, a relatively high supply voltage is always necessary in the output stage of the driver. However, the supply voltage can be lowered depending on the required bias and modulation voltage (set by I_{BIAS} and I_{MOD} respectively). In this design a supply up to 4.5V was chosen (V_{cc2} in Fig. 3(b)). On the other hand it isn't necessary to use this (high) supply voltage across the entire IC. Other block can be supplied by a far lower voltage of 2.5V (V_{cc1} in Fig. 2). Secondly, the 50Ω that terminates the driver can be increased when the transmission line between the EAM and the driver is made shorter. By tightly integrating the EAM and the driver, the transmission line can become as short as 2.5mm. An increased output impedance, R_{BT} , of 250Ω was chosen, which allows for a lower modulation and bias current, I'_{MOD} and I'_{BIAS} , in the driver to achieve the same bias and modulation voltage. This reduces the power consumption by 35% for an output swing of 2.5V_{pp}. Increasing R_{BT} further would deteriorate the signal quality due to reflections, while it would only reduce the power consumption marginally. Note that this technique is only possible in case the driver is DC-coupled to the EAM. Using an AC-coupled output would make the supply voltage grow with increasing output impedance in order to maintain sufficient headroom. Also broadband bias-tees were avoided since their sizes are too large to be used in the 10 channel array, both on- and off-chip.

Finally, the power consumption wasted in the left arm of the differential pair is reduced by using a third power supply, V_{cc3} , of 1.8V. This provides a power reduction of 20%. Careful modeling of the assembly and the on-chip/off-chip interconnections allowed to co-simulate the driver circuits with various parasitic elements and the EAM equivalent model in order to optimize the signal quality at strongly reduced power consumption.

4. Experimental results

The 10 channel x 11.3Gb/s EAM driver IC was fabricated in a 0.13μm SiGe BiCMOS process. Fig. 4 shows its die micrograph. The array of 10 separate drivers is clearly visible. The SPI-register can be seen on the lower left side, with the data path running from bottom to top. The total chip area is $5.5 \times 1.3\text{mm}^2$, which is determined by the 500μm pitch between the 10 EAM channels and the number of I/O pads. This gives sufficient room for on-chip decoupling capacitances, which is more than 2.5nF for each power supply.

Fig. 4. EAM driver array IC micrograph.

Fig. 5(a) shows the measured optical eye diagram at a data rate of 10Gb/s using a commercially available 10 Gb/s EAM. An extinction ratio of 8dB was measured with a $2^{31}-1$ pseudo random bit sequence (PRBS), consuming as little as 173mW on-chip, while reaching an output voltage swing of $2.5V_{pp}$ with a bias voltage of 1.7V.

Fig. 5. Output signal ($2^{31}-1$ PRBS): (a) Optical, (b) Electrical (0.5 V/div, 20 ps/div).

Measurement result of an electrical eye diagram, with a 50Ω oscilloscope as load instead of the EAM, is shown in Fig. 5(b). This was measured at the output of the EAM driver at a data rate of 11.3Gb/s and using a $2^{31}-1$ PRBS sequence. A 20-dB attenuator was added to avoid overloading the high-speed oscilloscope. Multiple adjacent channels were measured to check the influence of crosstalk, which was negligible. With a differential input voltage of $600mV_{pp}$ and a supply voltage of 4.5V a swing of $2.5V_{pp}$ was achieved consuming only 188mW on-chip and 31mW in the external 50Ω , resulting in a total power consumption of 219mW per channel. The 20-80% rise/fall times are 24 and 31ps respectively. The measured output jitter is $18.3ps_{pp}$ and $2.45ps_{rms}$, using a data generator with the measured jitter of $14.6ps_{pp}$ and $2.25ps_{rms}$. Also the pulse width control operates adequately and the programmable crossing point can be adjusted between 38.6% and 59.4% in 8 steps, as shown in Fig. 6.

Fig. 6. Pulse width control, (a) minimum, (b) maximum ($2^{31}-1$ PRBS, 0.5V/div, 20ps/div).

5. Power consumption discussion

A comparison with the power consumption of previous works is shown in Table. 1. (Note that it isn't always clear whether the papers only report the on-chip power consumption or also include the dissipation in the external resistor.) This table only contains single drivers, except for our presented work. The lowest power consumption reported was 470mW, which shows that this work is 50% below the state of the art. Even though reference [7] had twice the power consumption and the data rate was 10 times lower than the rate in this work, its output swing is considerably higher. By using the techniques reported here, a swing of 3.9V would give a power consumption of 405mW. Note that reference [7] didn't use a resistor R_{BT} , which corresponds to the technique of increasing it (to infinity). If this was done in this work, the power consumption would decrease to 335mW which was almost 30% below the reported consumption but at 10 times the data rate.

Reference [4] has a similar power/data rate, but only has a swing of $1V_{pp}$. If this work would be designed for a swing of $1V_{pp}$, the power consumption would be below 90mW. This gives a power/data rate that is less than 40% of reference [4].

Table 1. Power consumption comparison

Ref	Power (mW)	Data rate (Gb/s)	Output Swing (V_{pp})
[3]	980	10	2
[4]	850	40	1
[5]	800	10	4.5
[6]	675	10	2
[7]	470	1.25	3.9
This work	220 x 10	11.3 x 10	2.5

Fig. 7 shows the range of output swings and output bias voltages together with their corresponding power consumptions. It shows that the power consumption can be as low as 200mW for a swing of $2.4V_{pp}$ and below 300mW for a swing of $3V_{pp}$. It increases considerably when the bias voltage across the EAM goes up, even though the swing remains the same, especially at higher modulation voltages. This can partly be designated to the increase of the supply voltage, but it is mostly due to the increase of the bias current. Note that a great portion of this rise in power consumption is consumed in the external 50Ω . In the case of a 3V output swing the power consumption grows from 288mW to 401mW for minimum to maximum bias, which corresponds to an increase of 113mW or 40%. The power consumption in the external 50Ω grows from 45mW to 92.5mW, which is a difference of 47.5mW or 42% of the total increase. This points out that the on-chip power and heat generation isn't that profound, making a coolerless operation still possible.

It should be noted that the power consumption can be decreased even further when the modulator is closely integrated with the driver and the back termination resistor, R_{BT} , can be omitted, as discussed earlier. In this way a reduction of about 15% can be achieved, depending on the swing and biasing. Another possibility to decrease the consumption is to increase the external resistor in parallel with the EAM modulator. Changing the 50Ω into 66Ω would also give a reduction of 15%.

Fig. 7. Reach of the modulation and bias voltage with the corresponding power consumptions.

6. Conclusion

We have presented results of an ultra low power 10-channel EAM driver array with an output voltage up to $3V_{pp}$ at a total of 113Gb/s for OLT TX arrays in WDM-PON applications. The power consumption is below 220mW per channel, which makes coolerless operation possible, while the eye diagram measurements revealed excellent signal quality.

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