Experiments on 10Gb/s Fast Settling High Sensitivity Burst-Mode Receiver with On-Chip Auto-Reset for 10G-GPONs [Invited]

Xin Yin, Xing-Zhi Qiu, Jan Gillis, Jasmien Put, Jochen Verbrugghe, Johan Bauwelinck, Jan Vandeweghe, Heinz Krimmel, Dora van Veen, Peter Vetter, and Frank Chang

Abstract—This paper presents a 10Gb/s APD-based DC-coupled burst-mode receiver (BM-RX) with on-chip auto-reset generation and multiple data rates support, designed for 10G-GPONs. Record short 2R settling time of 75 ns (150 ns for multi-rate operation), high sensitivity of -31.3 dBm and large loud/soft ratio of 25.3 dB are demonstrated in burst-mode operation at 2.5G/5G/10Gb/s.

Index Terms—Passive optical networks (PON); 10G-GPON; burst-mode receiver (BM-RX); Fiber optics links and subsystems.

I. INTRODUCTION

Bringing the fiber-optic network closer to the home is a natural step in the migration process towards higher access bandwidth [1]. Passive optical networks (PONs) are one of most massively deployed optical access systems because of low cost and high-bandwidth provision. In PON systems, as shown in Fig. 1, multiple optical network units (ONUs) at the customer sides share the fiber plant and an optical line terminal (OLT) located at the central office. While downstream data are broadcasted in continuous-mode signals, the upstream data are transmitted in burst-mode and combined using a time division multiple access (TDMA) protocol.

A major challenge for next generation passive optical networks (NG-PONs) is the realization of a set of 10Gb/s burst-mode physical medium dependent (BM-PMD) components, namely a burst-mode transmitter (BM-TX) at the subscriber ONU, and a burst-mode receiver (BM-RX) as well as burst-mode clock and data recovery (BM-CDR) at the OLT of the PON system. Among these BM-PMD components, the 10Gb/s BM-RX is most challenging to design. It requires fast RX settling, to allow for a short burst preamble and hence high interactivity and throughput, combined with a high sensitivity and a wide dynamic range, to be compliant with installed optical distribution networks (ODNs), and to support flexible network deployment. Recently both AC-coupled and DC-coupled BM-RXs have been reported for IEEE 802.3av 10G-EPONs [2][3], but these require 64B/66B line coding and a relatively long RX settling time. Though FSAN has only

Fig. 1. PON system and upstream data link.

endorsed XG-PON1 with asymmetrical 10/2.5 Gb/s transmission rates so far, a first symmetrical XG-PON with 10/10 Gb/s has been reported in [4]. The BM-RX reported in [4] is an AC-coupled design that still requires a total settling time of 360 ns including CDR. A DC-coupled design however can achieve a much shorter RX settling time at the PON physical layer [5]. Moreover, a BM-RX allowing multi-rate operation is challenging to design for 10G-GPON systems because only scrambled NRZ is used without any line coding. In this work, we demonstrated the performance of a newly developed 10Gb/s APD-based BM-RX originally designed for symmetric 10G-GPON operation. It can process burst signals at 2.5G/5G/10Gb/s simultaneously without needing an external reset signal.

II. REALIZATION OF THE 10GB/S BM-RX

Fig. 2 shows the block diagram of the 10Gb/s APD-based DC-coupled BM-RX. A burst-mode transimpedance-amplifier (BM-TIA) is DC-coupled with a burst-mode limiting-amplifier (BM-LA).

A. 10Gb/s BM-TIA

The BM-TIA performs fast gain setting in three steps (High gain, Medium gain and Low gain) by means of a variable-gain TIA core followed by a variable-gain single-ended-to-differential (S2D) circuit. Ref. [6] proposed a 1.25Gb/s TIA core with three feedback resistors in parallel using two nMOS switches. At 10Gb/s, the parasitics introduced by these additional feedback paths would limit the TIA frontend bandwidth. To make sure that the circuit is stable and peaking remains within specifications, ref. [7]

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X. Yin, X.-Z. Qiu, J. Gillis, J. Put, J. Verbrugghe, J. Bauwelinck and J. Vandeweghe are with Ghent University, INTEC/IMEC, Sint-Pietersnieuwstraat 41, 9000 Gent, Belgium (e-mail: xin.yin@intec.ugent.be).

H. Krimmel is with Alcatel-Lucent, Bell Laboratories, Lorenzstr. 10, 70435 Stuttgart, Germany.

D. van Veen and P. Vetter are with Alcatel-Lucent, Bell Laboratories, 600 Mountain Ave, Murray Hill, NJ 07974, USA.

F. Chang is with Vitesse Semiconductor Corporation, Transport Systems Engineering, 741 Calle Plano, Camarillo, CA, USA.

Fig. 2. The block diagram of the 10Gb/s DC-coupled BM-RX with on-chip auto-reset generation and activity detection.

switches the open-loop gain by varying the load resistor at the input stage, but this further complicates the gain-bandwidth tradeoff inside the TIA core. In this design, the 2nd gain switching is done by a load impedance switch in S2D. This implementation is advantageous over [6]. It simplifies the gain-bandwidth tradeoff as the noise of the S2D stage is less critical, allowing optimal bandwidth. As the gain-switching in the S2D stage has an open-loop behavior, stability is of no issue, resulting in a reliable and faster response.

A dummy TIAD generates the references for both the S2D and the gain switch block. When a burst has ended, the BM-TIA is reset to high transimpedance gain for maximum RX sensitivity. When a new incoming burst exceeds a certain power threshold, the transimpedance switches to Medium gain, and is possibly further reduced to Low gain, all within a few nanoseconds, under the control of logic signal GS1 and GS2. Once set, the TIA transimpedance gain is locked and kept constant during the burst payload. Such fast gain settling (<10 ns) can only be achieved by a BM-TIA using a reset signal to wipe any remembrance of the preceding burst [8]. Fig. 2 indicates that the BM-TIA has no reset pin. The reset signal is available in the subsequent BM-LA, and conveyed to the BM-TIA via common-mode signaling. The input stage of the BM-LA alters the common-mode voltage of the BM-TIA output. The BM-TIA extracts an on-chip reset signal out of these common-mode changes.

B. 10Gb/s BM-LA

The 10Gb/s BM-LA is a DC-coupled feedback-type RX. It implements a fast offset integrator with two switchable time constants as shown in Fig. 2. When a new burst arrives, the BM-LA first performs fast offset compensation and amplitude recovery with a short time constant. Once the correct threshold is established, the offset integrator switches to a larger time constant and enters a slow tracking mode, which is critical to provide a higher tolerance to consecutive identical digits (CIDs) within the payload. The DC-coupled fast response BM-LA needs a reset signal. In these experiments, the reset signal can be provided externally by the system, or generated internally by the BM-LA chip itself (auto-generated). In the latter case the BM-LA itself detects the end of a burst, resets the decision threshold to an initial

Fig. 3. (a) A typical G-PON OLT line card configuration; (b) the proposed 10G-GPON BM-RX eliminates the need for the time-critical feedback signals from the MAC layer.

state, and waits for the arrival of a next burst. As soon as new burst activity is detected on chip, it quickly enables the offset compensation loop to extract the decision threshold.

C. On-chip Auto Reset Generation

To ensure high uplink transmission efficiency in PONs, a short inter-burst guard time and settling time are required for BM-RXs. In this case, a reset signal is used to erase all information from the previous burst and prepare the

BM-RX for the newly coming burst. As shown in Fig. 3(a), this reset signal usually originates from the media access control (MAC) layer which knows arrival and end times of bursts from all ONUs. Removing this external reset signal greatly simplifies the interface between physical and MAC layer and enables the use of the BM-RX in reamplification, regeneration and retiming (3R) nodes where no such timing information is available. So it is beneficial if the BM-RX itself (so the physical layer) is capable of detecting when the burst signal ends and generating internal reset signal as shown in Fig. 3(b). In this case, no time-critical control interfaces cross the barrier between PHY and TC layer which is a real advantage in terms of interoperability.

The auto-reset generation have to be designed to accommodate new requirements of next generation PONs. As it is important that the NG-PONs maintain compatible with existing ODN, a FEC code is mandatory in 10G/10Gb/s symmetric PONs in order to meet its optical power budget requirement [9]. This implies that the auto-reset generation should be tolerant to possible higher bit error rate (BER) in the link. Our previous work [10] generates a on-chip reset signal based on measuring the time since the last received '1'. This duration is chosen sufficiently longer than the maximum CID in order to avoid an untimely reset signal during the payload. However, the auto-reset generation will suffer from noise, especially at the high pre-FEC BER. A better algorithm has been proposed in [11], instead of restarting the counter after a 1-bit fault, we could tolerate a number f faults before the counter restarts again. The idea is to generate a reset signal after receiving n consecutive bits, including a maximum of f 1-bits for high BER case.

The implementation of the on-chip auto-reset generation is shown in Fig. 4, using a clock counter and a data counter. Every time that the data counter exceeds its threshold (f), the EoB detection is restarted. On-chip auto-reset is generated after the clock counter exceeds the clock threshold (n). In this case the probability of missing the EoB is [11],

$$P_{EoB}(k) = \begin{cases} 0 & \text{if } k < n \\ P_n & \text{if } k = n \\ P_{EoB}(k-1) + P_r(k-n) \cdot P_n & \text{otherwise} \end{cases} \quad (1)$$

where $P_{EoB}(k)$ is the probability of missing the EoB within k bits after the end of the preceding burst, and P_n is the probability of receiving n consecutive 0-bits during the guard time. $P_r(k)$ is the probability that the counter is restarted after exactly k bits, which happens when the k^{th} bit is detected as a logic 1 and EoB was not detected before. Taking into account the time needed to restart the counter, expressed as r bit periods, $P_r(k)$ is equal to,

$$\begin{cases} 1 & \text{if } k = 0 \\ 0 & \text{if } 0 < k < f + r + n \\ \sum_{Nr=N1}^{Nr=N2} Div(k-r \cdot Nr, Nr) & \text{otherwise} \end{cases} \quad (2)$$

$\times BER^{Nr \cdot (f+1)}$
 $\times (1 - BER)^{k - Nr \cdot (r+f)}$

where Nr is the number of times the counter restarts during the EoB-detection, $N1 = \lfloor \frac{k}{n+r-1} \rfloor$, and $N2 = \lfloor \frac{k}{f+r} \rfloor$. $Div(k, pl)$ is thus the number of possible divisions of k bits over pl places ($pl \geq 1$) with f ones and maximally $n-1$ bits in each place and is given by,

Fig. 4. Implementation of on-chip auto-reset generation.

$$Div(k, pl) = \begin{cases} C_k^f & \text{if } pl = 1 \\ \sum_{k'=k1}^{k'=k2} C_k^f Div(k-k', pl-1) & \text{if } pl > 1 \end{cases} \quad (3)$$

where C_k^f is the number of f -combinations from a given set of k elements, $k1 = \max[f, k - (pl-1) \cdot (n-1)]$, and $k2 = \min[n-1, k - (pl-1) \cdot f]$.

As shown in Eq. (1), (2) and (3), the probability of missing the EoB is strongly dependent on n and f . Therefore, both clock counter (n) and data counter (f) are designed to be fully programmable, which makes the auto-reset generation flexible and robust to use for different BER scenarios.

D. Mutli-Rate Operation

An OLT optionally supporting multi-rate operation can be advantageous because of backward compatibility and possible smooth upgrade path from existing PON networks. In 10G-EPON upstream, the BM-RXs operate in dual-rate 1G/10G burst-mode reception mode for 8B/10B coded 1.25Gb/s and 64B/66B coded 10.3125Gb/s bursts [9]. The specified line code forces that the maximum CID has similar length in time for both 1G and 10G upstream bursts, which relaxes the time-constant design trade-off if the AC-coupling method is used [11]. However, the line code used in 10G-EPON contributes additional overheads (20% at 1G and 3% at 10G) and reduces the upstream transmission efficiency. Furthermore, the dual-rate BM-RX in [2] uses two BM-LAs: one for 1G and another for 10G, which increases the PMD complexity and cost.

To improve the upstream efficiency and reduce the cost, it is desirable to allow multi-rate operation for only scrambled NRZ data with a single BM-RX. The main technical challenge is to keep the short settling time of the BM-RX while tolerating a very long sequence of CID because of the multi-rate operation. For example, the 1-bit duration of 2.5Gb/s data is 4 times of the bit duration of 10Gb/s data, which implies the possible maximum CID length at 2.5Gb/s is 4 times longer as well. Because the proposed BM-RX has two operation modes with different time constant in the offset compensation loop, it can achieve simultaneously a fast response and a large CID tolerance. Assuming the maximum CID of scrambled NRZ is about 72 bit, the BM-RX need to handle 7.2 ns long CID at 10Gb/s but more than 28.8 ns for 2.5Gb/s data. In this implementation, the offset integrator was designed to have a large time constant during

Fig. 5. The 10Gb/s BM-PMD components for 10G-GPON upstream experiments.

payload to allow at least 51.2 ns CID without significant output jitter deterioration, which makes it suitable for multi-rate operation without extra line coding overheads.

III. INTEGRATION OF THE 10Gb/s BM-PMD COMPONENTS AND EXPERIMENTAL RESULTS

New 10Gb/s BM-TIA and BM-LA components, fabricated in a 0.13 μm SiGe BiCMOS process, were integrated as shown in Fig. 5. To emulate the uplink PON system, two 1.3 μm burst-mode transmitters (BM-TXs) are alternately sending 10Gb/s bursts upstream. BM-TX1 is electro-absorption modulator laser (EML) based, it has an output power of +4.4 dBm and an extinction ratio (ER) of 10 dB. BM-TX2 is a DFB laser based TOSA, it has an output power of -0.8 dBm with an ER of 7 dB. The two TX outputs are combined by a 2x2 splitter, and fed to the BM-RX. The BM-RX is AC coupled to the BM-CDR board providing clock and data recovery.

We first evaluated the BM-RX on its own, with an external reset signal. The 10Gb/s burst packets consisted of a 76.8 ns preamble and a 1280 ns payload. The guard time between bursts was set to 25.6 ns. The payload was composed of a non-return-to-zero (NRZ) $2^{31}-1$ pseudo random bit sequence (PRBS) data pattern plus CID patterns with 72 bits of successive 1s resp. 0s. The APD multiplication factor M was set to 9. Fig. 6 shows the BER curves measured with an external reset signal. The measured input sensitivity of the BM-RX at a pre-FEC BER of 10^{-3} was -31.9 dBm for burst-mode back-to-back (BM-B2B). With 2 branches of BM-TXs, the BM-RX sensitivity measured on the weak packet emitted by BM-TX1 was -31.3 dBm for the worst case when the output power of BM-TX2 equals -6 dBm. The error-free input overload level was found to be higher than -5 dBm. This yields a dynamic range of more than 26.3 dB. The BM-

Fig. 6. The measured BER curves for BM-B2B and 2 TX branches.

RX was also assessed in different loud/soft ratios and the measured BM-RX penalties due to the preceding loud burst are shown in Fig. 7. The maximum BM penalty was only 0.6 dB at a loud/soft ratio of 25.3 dB.

Fig. 8 shows the measured BERs using the BM-RX with the BM-CDR. The preamble time was increased up to 150 ns to accommodate the CDR settling time. The input sensitivity at pre-FEC BER of 10^{-3} remains unchanged when the BM-RX is followed by the BM-CDR. The BM-RX output thus provides already an almost ideal 2R-regenerated signal to the CDR.

We finally evaluated the BM-RX at different upstream

TABLE I
PERFORMANCE SUMMARY

	IEEE Std 802.3av [12]	This work
AC/DC coupling	AC	DC
Rx settling (ns)	800	75/150 (multi-rate)
Sensitivity at BER= 10^{-3} (dBm)	-28	-31.3
Dynamic range (dB)	≥ 22	≥ 26.3
Line code	8B/10B for 1.25Gb/s; 64B/66B for 10.3Gb/s	Scrambled NRZ (no extra line coding overheads)
Multi-rate operation	1.25G/10.3Gb/s	2.5G/10Gb/s
Reset signal	AC coupling without reset signal	Auto-reset generation

Fig. 7. BM penalty versus different loud/soft ratio.

Fig. 9. Measured BER curves at 2.5G/5G/10Gb/s in BM with and without an external reset signaling.

Fig. 8. Measured BER curves using BM-RX with BM-CDR.

data rates with on-chip auto-reset generation. In this experiment, the BM-TX2 operated at a data rate of 10Gb/s while the BM-TX1 was sending bursts at 2.5G, 5G and 10Gb/s respectively. For auto-reset and multiple-rate operation, the guard time and settling time were increased to 100 ns resp. 150 ns. The guard time up to 1 ms was also tested with on-chip auto-reset and the BM-RX works properly. The payload remains NRZ $2^{31}-1$ PRBS pattern plus CID patterns with 72 bits of 1s resp. 0s for different data rates. The measured BER curves are shown in Fig. 9. At 10Gb/s, the RX sensitivity penalty from using on-chip auto-reset generation instead of

an external reset signal is limited to 0.3 dB at pre-FEC BER of 10^{-3} . For 2.5Gb/s operation we assume there is no strong FEC, and therefore the BER threshold was set to 10^{-10} . At this BER threshold the sensitivity penalty of using on-chip auto-reset is negligible for 2.5Gb/s operation. With auto-reset generation, an upward deviation of the BER curve is found when the input power is lower than -31 dBm. This is attributed to the fact that input signals less than -31 dBm are too weak for the on-chip auto-reset circuit in our current design, which targets supporting Class N2 optics defined for the XG-PON. A detailed summary of the BM-RX performance is outlined in Table I.

IV. CONCLUSION

An advanced DC-coupled BM-RX with on-chip auto-reset generation and multi data rate support was designed for symmetrical 10G-GPON systems. Our BM-RX realized a short 2R settling time, a high sensitivity and a large loud/soft ratio with multi-rate operation. In the experiment, we achieved an excellent sensitivity of -31.3 dBm for weak/strong bursts at 10Gb/s, with a very short 2R RX settling time of 75 ns. Moreover, to achieve high interoperability and backward compatibility, auto-reset generation and multi-rate operation has been investigated and incorporated into the newly developed BM-RX. We demonstrated experimentally the BM-RX can process burst signals at 2.5G/5G/10Gb/s simultaneously without needing an external reset signal. It shows a great potential for use in emerging

symmetric 10G-GPON systems and allows for more flexible future optical access networks.

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REFERENCES

- [1] A. Shami, M. Maier, and C. Assi, *Broadband Access Networks: Technologies and Deployments*, ser. Optical Networks. Springer, 2009.
- [2] K. Hara, S. Kimura, H. Nakamura, N. Yoshimoto, and H. Hadama, "Ultra fast response AC-coupled burst-mode receiver with high sensitivity and wide dynamic range for 10G-EPON system," *IEICE Transactions*, vol. 94-B, no. 7, pp. 1845–1852, 2011.
- [3] M. Noda, S. Yoshima, K. Ishii, S. Shirai, M. Nogami, and J. Nakagawa, "Dual-rate optical transceiver incorporating fully optimized burst-mode AGC/ATC functions for 10G-EPONs systems," in *Optical Communication (ECOC), 2010 36th European Conference and Exhibition on*, sept. 2010, pp. 1–3.
- [4] D. van Veen, D. Suvakovic, M. F. Lau, H. Krimmel, A. de Lind van Wijngaarden, J. Galaro, J. Dungee, B. Farah, S. Corteselli, B. Weeber, R. Tebbe, D. Eckard, J. Smith, J. Bouchard, J. Kotch, and P. Vetter, "Demonstration of a symmetrical 10/10 Gbit/s XG-PON2 system," in *Optical Fiber Communication Conference and Exposition (OFC/NFOEC), 2011 and the National Fiber Optic Engineers Conference*, march 2011, pp. 1–3.
- [5] X. Yin, X. Qiu, J. Gillis, J. Put, J. Verbrugghe, J. Bauwelinck, J. Vandewege, F. Blache, D. Lanteri, M. Achouche, H. Krimmel, D. van Veen, and P. Vetter, "Dc-coupled burst-mode receiver with high sensitivity, wide dynamic range and short settling time for symmetric 10G-GPONs," in *Optical Communication (ECOC), 2011 37th European Conference and Exhibition on*, sept. 2011, pp. 1–3.
- [6] M. Nakamura, Y. Imai, Y. Umeda, J. Endo, and Y. Akatsu, "1.25-Gb/s burst-mode receiver sICs with quick response for PON systems," *Solid-State Circuits, IEEE Journal of*, vol. 40, no. 12, pp. 2680–2688, dec. 2005.
- [7] S. Nishihara, M. Nakamura, T. Ito, T. Kurosaki, Y. Ohtomo, and A. Okada, "A SiGe BiCMOS burst-mode transimpedance amplifier using fast and accurate automatic offset compensation technique for 1G/10G dual-rate transceiver," in *Bipolar/BiCMOS Circuits and Technology Meeting, 2009. BCTM 2009. IEEE*, oct. 2009, pp. 158–161.
- [8] Y. Ohtomo, H. Kamitsuna, H. Katsurai, K. Nishimura, M. Nogawa, M. Nakamura, S. Nishihara, T. Kurosaki, T. Ito, and A. Okada, "High-speed circuit technology for 10-Gb/s optical burst-mode transmission," in *Optical Fiber Communication (OFC), collocated National Fiber Optic Engineers Conference, 2010 Conference on (OFC/NFOEC)*, march 2010, pp. 1–3.
- [9] K. Tanaka, A. Agata, and Y. Horiuchi, "IEEE 802.3av 10G-EPON standardization and its research and development status," *Lightwave Technology, Journal of*, vol. 28, no. 4, pp. 651–661, feb.15, 2010.
- [10] C. Melange, X. Yin, B. Baekelandt, T. De Ridder, X.-Z. Qiu, J. Bauwelinck, J. Gillis, P. Demuytere, and J. Vandewege, "Fully DC-coupled 10Gb/s burst-mode pon prototypes and upstream experiments with 58ns overhead," in *Optical Fiber Communication (OFC), collocated National Fiber Optic Engineers Conference, 2010 Conference on (OFC/NFOEC)*, march 2010, pp. 1–3.
- [11] J. Put, X. Yin, X. Qiu, J. Gillis, J. Verbrugghe, J. Bauwelinck, J. Vandewege, F. Blache, D. Lanteri, M. Achouche, H. Krimmel, D. van Veen, and P. Vetter, "Dc-coupled burst-mode receiver with high sensitivity, wide dynamic range and short settling time for symmetric 10G-GPONs," *Opt Express*, vol. 19, no. 26, pp. B594–603, 2011.
- [12] "IEEE Standard for Information technology - Telecommunications and information exchange between systems - Local and metropolitan area networks - Specific requirements Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications Amendment 1: Physical Layer Specifications and Management Parameters for 10 Gb/s Passive Optical Networks," 2009.

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Xin Yin received the Ph.D. degree in electronic engineering from Ghent University, Belgium in 2009. Since 2007, he has been a researcher of IMEC INTEC/Ghent University. His research interests include high-speed opto-electronic circuits and transmitter/receiver subsystems, with emphasis on burst-mode receivers and clock data recovery ICs for optical access networks.

Xing-Zhi Qiu (M'98) received her Ph.D degree in Electronics Engineering from Ghent University, Gent, Belgium in 1993. She gained 25 years R&D experience within INTEC in the field of high speed physical layer hardware design, mostly for advanced broadband telecommunication systems and in particular for high speed optical access networks. She has been strongly involved in many EU-funded projects, and managing analog/digital chip design and sub-system development within the group. She co-authored more than 130 publications on high speed chip and telecom system design, and 6 patents on communications.

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Jan Gillis received his electrical engineering degree from KaHo Sint-Lieven, Belgium, in 2000. In August 2000, he joined the INTEC_Design group, where he is involved in optical testing and analog layout.

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Jasmien Put was born in Herentals, Belgium, in 1984. She received the engineering degree in electronic circuits and systems in 2007 from Ghent University, Belgium. In 2007 she joined the INTEC_design laboratory where she was working towards the Ph.D. degree. Her research is focused on the design of opto-electronic integrated receiver circuits.

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Jochen Verbrugghe received the M.Sc. degree in computer science in 2007 and the M.Sc. degree in electrical engineering in 2009 from the University Ghent (UGent), Belgium. In September 2009, he joined the INTEC_Design group. His main interest is analog circuit design.

Peter Vetter is Department Head for Access Systems in Bell Labs Murray Hill. He received the degree of Physics Engineer from Gent University (Belgium) in 1986 and a PhD in 1991. After a post-doctoral fellowship at Tohoku University (Japan), he joined the research centre of Alcatel (now Alcatel-Lucent) in Antwerp in 1993. He subsequently worked on liquid crystal displays, optical interconnections, optical access, access platforms, and access network architectures, first as researcher

and later as department manager. In 2000, he became a founding member of an Internal Venture and R&D leader for the PON technology that produced the first FTTH product in Alcatel. He also initiated and managed activities in various European Research Projects. From 2004-2008, he was the overall project manager of IST MUSE, a major European integrated project with 36 partners and covering all aspects of broadband access. Since 2009, he works at Bell Labs in Murray Hill, New Jersey, where he leads research on optical access, access platforms, and energy efficient access networks.

He has authored or co-authored more than 60 international papers, including several invited. He has served in the technical programme committees of ECOC, NOC, and BB Europe. He is also the chair of the Wireline Access Working Group in GreenTouch.

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Johan Bauwelinck was born in Sint-Niklaas, Belgium, in 1977. He received the engineering degree in applied electronics and a Ph.D. degree in applied sciences, electronics from Ghent University, Ghent, Belgium, in 2000 and 2005, respectively. He has been a research assistant in the INTEC_design Laboratory, Ghent University, since 2000 and he is currently a full-time tenure track professor. His research focuses on high-speed, high-frequency (opto-) electronic circuits and

systems.

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Jan Vandewege was born in Ghent, Belgium in 1949, and holds Master and Ph.D. degrees in Electronics Engineering from Ghent University (UGent). His interests include fast analog electronics, Surface Acoustic Wave devices, fibre optics and Si and GaAs integrated circuits. In 1985 he created INTEC_design, a research and Ph. D. training lab for electronics design engineers, tackling analog design problems involving high speed, burst mode, and hard real time operation. INTEC_design

started 155Mbps PON research in 1991, and is now concentrating on 10Gbps burst-mode communication and on large scale gigabit optical access. Full professor at UGent, he enjoys guiding an international team of researchers, and stimulating creativity in a hands-on, real world approach.

Frank Chang is currently Principal Engineer, Systems at Vitesse Semiconductors Corp principally specializing in optical system engineering and IC product specifications and definition issues for telecom, datacom and PON access markets. Previously he worked as individual contributor and project manager roles at JDS Uniphase, Cisco/Pirelli, and Mahi Networks for the development of WDM systems, linecards, and fiber optics components. He has coauthored over 80 peer-reviewed journal and

conference articles, contributed to two book chapters and represents Vitesse at standard organizations including the OIF/ITU-T, IEEE802.3, FSAN, and Ethernet Alliance. He has been serving as the member of the technical program committee for OFC/NFOEC for many years in a row and a number of other international conferences. He holds a Ph.D degree in Optoelectronics from the University of Montreal, and is Senior Member of IEEE/LEOS and OSA.

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