Towards Reel-to-Reel Integration of Ultra-Thin Chips to Polymer Foils

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Abstract

The EU FP7 funded project Chip2Foil aims to realise a technology platform allowing a radically different implementation of the assembly process for ultra-thin chips (UTCs) to polymer foils. The process is based on redistribution of the tolerance budget, and consists of two major steps: self-assembly supported chip placement followed by an adaptive circuitry approach for realising the electrical interconnects. The concept accepts non-contact, low precision presentation of a UTC to the self-assembly force field, which brings the chip to a final position with moderate precision. Next, in an adaptive interconnection process the chip position is measured with respect to the circuitry on the foil and interconnects are created on an individual chip and IO basis. The main technology building blocks are described and the current performance is demonstrated, including chip thinning, fast UTC release from wafer tape, self-assembly supported chip placement using magnetic forces and adaptive electrical interconnection by laser scribing of a screen-printed silver patch.

Introduction

The chip placement industry has developed into a mature industry. Impressive performance levels are achieved. Industrial chip placement processes reach throughput levels of 10k placements per manipulator per hour and higher, and achieves 3 σ repeatability levels even below 10 μ m, depending on throughput levels. A very common process is the placement of Surface Mount Devices (SMDs) on a rigid PCBs; the components are placed on solder pads and electrical connections and mechanical bonding involves passing the PCB through a solder reflow process. Also, naked die are placed on a lead frame or substrate, either with the pads facing upwards for wire bonding or facing down in flip-chip assembly. Direct placement of a naked die on a rigid or flexible printed circuit board, so called direct chip attach or chip-on-board, is being used on an industrial scale, albeit only for low IO counts (RFID) or in niche markets.

New package form factors, however, ask for the development of new or adjusted solutions to the chip placement and interconnection process. One example are foil-based smart electronic packages that are currently emerging [1]. The bendability of polymer foil-based electronic packages offers design freedom to integrate them into a variety of structures, instruments and devices. The package cost can be very low in particular when produced in a reel-to-reel scenario.

Because of compliancy with the bendability of the package and the wish to hide the electronics, there is a need to integrate ultra-thin components. The integration of such components introduces new challenges, which originate in the very low thickness and resulting chip flexibility, the brittleness and edge effects (defects leading to damage and failure).

This paper reports on the development of a complete process flow for ultra-thin chip (UTC) assembly to polymer foils leading to the manufacturing of low-cost packages, which is the target of the EU FP7 funded project Chip2Foil. The Chip2Foil process is based on redistribution of the tolerance budget, and consists of two major steps: a self-assembly supported chip placement approach followed by an adaptive circuitry approach for realising the electrical interconnects between the chip and the circuitry on the foil.

The remainder of this paper introduces the Chip2Foil process and technology. First, the specific case focused on, a communicative foil-based package for Smart Blister applications, is described. Then the Chip2Foil process flow is introduced, followed by a description of the main technology building blocks. Reel-to-reel implementation issues are discussed and finally conclusions are presented.

Communicative foil-based packages for Smart Blisters

The current case focuses on communicative foil-based packages. Such packages provide increased interaction between a user and a packed product, e.g. to support identification and authentication, traceability and monitoring the quality of the packed product. Applications can be found in amongst others food, health and logistics. A specific example is a sensor foil which is added to the lidding foil of a standard medicine blister to create a Smart Blister in support of therapy compliance, see Fig. 1.

Fig. 1. Lab-based realisation of a Smart Blister package prototype, example of a communicative foil-based package to support therapy compliance. In this prototype, packaged chips and other components are manually placed and bonded to the foil. (Courtesy Qolpac BV and Holst Centre, The Netherlands).

Therapy non-compliance is a pressing ethical and economic issue. In a 2003 study, the World Health Organization underlines the importance of adherence to therapies, and quotes: “Increasing the effectiveness of adherence interventions may have a far greater impact on the health of the population than any improvement in specific medical treatments” [2]. The Smart Blister is an electronic compliancy aid. Upon pushing through of a pill, an electrical resistor at the location of the push-through area in the Smart Blister is broken, which event is monitored and registered by the on-package chip. Data on these events is wirelessly communicated through Near Field Communication (NFC) to a mobile phone application, and can be accessed by a user, which is either the patient or a medical professional. Potentially, these packages are to be produced in very high volumes. If a very low cost assembly process and package can be realized, entirely new application domains may also be opened up, for instance in food logistics.

Process design and technology building blocks

Chip integration includes placement, mechanical bonding, encapsulation and electrical interconnection. The ultra-thin chips focused on have a size of approximately $1 \times 1 \text{ mm}^2$, a thickness of $15\text{-}20 \mu\text{m}$, and have in the order of 20 IO. UTCs can easily deform and get damaged in a contact-based assembly process, and release from a wafer tape and handling using a pick-up tool is complicated. Also, the chip is placed on a thin layer of die attach adhesive to mechanically bond the chip to the foil. An additional problem with a contact-based placement process of a UTC is that the adhesive can easily contaminate the top surface of the chip and subsequently the pick-up tool.

Self-assembly potentially offers a solution to this challenge. Self-assembly is the autonomous arranging and assembling of components using patterned force fields [3]. It contrasts with the classic approach to assembly which uses direct and controlled manipulation of usually single components. Self-assembly is in particular applied to the heterogeneous integration of small-scale devices, and has the potential to improve assembly process performance in terms of increased throughput because of massive parallelisation, improved alignment precision and reduced cost. Also, it offers the potential of handling and assembling small-scale objects which pose challenges for classic manipulation. In the Chip2Foil process, self-assembly is used for the non-contact trapping and alignment of the UTC.

The proposed overall Chip2Foil process flow is depicted in Fig. 2. The starting point is a foil which is provided with the required circuitry including breakable resistors. In the first step, chip assembly is done by directed presentation of the chip to within the working range of the self-assembly force field. The role of the self-assembly process is to bring the chip to a position within the allocated chip area, but with moderate precision only.

Fig. 2. Assembly process sequence: (A) foil with circuitry (only the region around the location where the chip is to be assembled is shown with the contact pads of the circuitry on the foil), (B) self-assembled chip with moderate precision, and (C) realized interconnects.

The bond pads of the chip are facing up, see Fig. 3. In the next step, the electrical interconnects are made on an individual chip and individual IO basis. The interconnection process involves measuring the chip position with respect to the foil circuitry followed by a fast and flexible laser machining-assisted interconnection process. The flexibility of the adaptive circuitry approach relaxes the demand on the self-assembly process. The exact position of the chip does have a limited effect on the total interconnect length to be realised. Translational and rotational position variations in the order of $\pm 300\text{-}500 \mu\text{m}$ and $\pm 15^\circ$ respectively can still be compensated for the selected circuit and chip design.

Fig 3. Chip layout and interconnection.

From a process design perspective, the performance potential of the proposed process is based on the redistribution of the tolerance budget and the combination of moderate precision self-assembly with adaptive interconnection. The self-assembly process is very tolerant in terms of the demand on the chip presentation process, i.e. the process which bring the chip in the working range of the self-assembly field. Similarly, the adaptive circuitry process is tolerant for the self-assembly process. Reducing tolerance limits for processes generally has a positive effect on the process performance in terms of cycle time and yield.

For the implementation of this process, a number of technology building block must be available. The circuitry on the foils, including the resistors in the push-through areas and the antenna for wireless communication, are realised by screen printing, which is an available technology. Energy will come from a laminated battery or from a chip with energy

harvesting functionality. The major technology building blocks focused on in the Chip2Foil project include:

- Chip thinning;
- Ultra-thin chip release from wafer tape;
- Ultra-thin chip placement and mechanical bonding;
- Ultra-thin chip encapsulation;
- Adaptive electrical interconnection.

Chip thinning

Thinning of silicon chips is widely applied on wafer level, where the whole wafer is thinned down to a thickness of about 100 to 150 μm in a chemical or mechanical way [4]. As part of the Chip2Foil project, a single chip thinning process for small chip ($1 \times 1 \text{ mm}^2$) was developed and optimized. Single chips with an original thickness of typically 500 μm are thinned down to a thickness of 20 μm and even lower.

The bare chips are mounted face down on a temporary glass carrier with a dedicated wax. The backside of the chips is then lapped on a glass plate with a slurry of Al_2O_3 and consecutively chemical-mechanical polished with a soft lapping cloth (PM5 Logitech Lapping & Polishing Machine). In previous work [5], protection of the edges of the chips was realized by mounting dummy chips around the functional chip. This is however not possible when the functional chips are very small because the handling of the chips during mounting becomes too complex. As an alternative, different types of wax were evaluated to hold the chip into place and to protect the chip edges at the same time. To realize the latter, the wax layer must be thick enough to reach the top of the chip edges to protect the edges during the lapping and polishing steps. Experiments showed that glycophtalate wax is a suitable candidate to fulfil the wax requirements. Fig. 4 shows pictures of single mounted chips (RF Nordic chips, $2 \times 2 \text{ mm}^2$) in glycophtalate wax. It is clearly visible that the wax is completely covering the chip edges. The slurry grains exert a relatively big force on the edges of the embedded chip, which is a difference compared to the process where dummy chips were placed around the functional chip. As a consequence, chips are subject to rounding at the edges. By optimizing the thinning process parameters (plate speed, weight applied, etc.), a flatness variation over the complete chip below 2 μm was achieved.

Fig. 4. Pictures of the single mounted die (RF Nordic chips $2 \times 2 \text{ mm}^2$) in glycophtalate wax.

The thinning process was further optimized by splitting the lapping step into two consecutive lapping steps with decreasing slurry grain sizes. The first lapping step decreases the chip thickness from its original thickness down to 100 μm with a removal rate of about 55 $\mu\text{m}/\text{minute}$ and the second

lapping step decreases the chip thickness from 100 μm down to 50 μm with a removal rate of about 20 $\mu\text{m}/\text{minute}$. By splitting up the lapping process, the final surface roughness and surface damage is minimized before the polishing step. This has proven to increase the yield of the chip thinning process.

Both purely mechanical polishing and electromechanical polishing were compared and evaluated. The final roughness of the backside of the chips after mechanical polishing is $0.65 \pm 0.13 \text{ nm}$ and after CMP $0.7 \pm 0.18 \text{ nm}$, measured with a non-contact optical profilometer on an area of $100 \times 100 \mu\text{m}^2$. Low surface roughness is important, since every roughness or damage feature on the backside of the thinned chips can be a seed for a fatal crack in the chip during subsequent and continuous bending of the chip.

Any functional chip has a certain amount of active layers at the top of the chip. Since the coefficients of thermal expansion of these active layers are never similar to the coefficient for silicon, large internal stresses in the chip can be expected, resulting in chip bow after thinning. Fig. 5 shows WYKO non-contact optical profilometer images of the top surface of a thinned RF Nordic radio chip after release from the temporary glass carrier. The chip is thinned down to a final thickness of 30 μm of which about 10 μm is made up by the active layers. The internal stresses result in a chip bow with a radius of curvature of 10 cm. The chip bow may present challenges during chip release and placement or create stress in the interconnections when flattened.

Fig. 5. Curvature of the top surface of a 30 μm thick chip ($2 \text{ mm} \times 2 \text{ mm}$). The difference between the green and red colour is about 10 μm

Ultra-thin chip release from wafer tape

UTCs introduce a difficulty in chip ejection, i.e. the release from wafer tape. In most industrially applied ejection methods, the chips are usually pushed from one side with a system of one or more needles and picked up from the other side by a pick and place tool. The flexibility of UTCs causes them to bend with the dicing tape, rather than coming loose. Also, chip breakage can occur due to concentrated contact stress between the needles and the brittle chip. As a consequence, ejection cycle times increase very much. Also, imperfections at the edge of the chip may propagate into

cracks and lead to brittle fracture if the stress level exceeds a critical value.

Several concepts for UTC ejection tools are known, see [6]. A number of ejection tools was experimentally investigated, including a multi-pin tool, a multi-stage tool, a membrane tool and a heated tool. All of these tools share the same basic idea of detaching the chip from the dicing tape: reducing the contact area between the chip and the tape while inducing the least possible stress into the chip. The multi-stage tool gives the best performance in terms of ejection cycle time and yield (number of undamaged chips). However, the tool is difficult to scale down to chips of a size of $1 \times 1 \text{ mm}^2$. The multi-pin ejection tool, see Fig. 6, offers good performance and allows scaling down to smaller chips. Depending on the chip size, a certain number of pins is suitable for chip ejection. For a $1 \times 1 \text{ mm}^2$ chips it was found that a single pin ejection tool is well suited.

Fig. 6. Multi-pin UTC ejection tool.

Ejection experiments with this tool were carried out using bare Si chip with thickness between 25 and $50 \mu\text{m}$ and ultra-thin diodes ($9.2 \times 5.44 \text{ mm}$, thickness $20 \mu\text{m}$, $40 \mu\text{m}$ and $60 \mu\text{m}$). The experiments showed ejection times of 100-200ms and yield levels better than 98%. Other experiments used the IZM41.1 chip in ejection trials ($0.9 \times 0.9 \text{ mm}$, $20 \mu\text{m}$ thickness). In total 400 chips were ejected and placed on a substrate. All chips were visually inspected for damage. A 100% yield was achieved, with an average ejection time of 46 ms (i.e. 21 chips per second).

Ultra-thin chip self-assembly placement and bonding

For the self-assembly process, magnetic force fields are used, see Fig. 7 for a sketch. Magnetic fields have a large working range. This allows non-contact presentation of the chip to the self-assembly field.

Fig. 7. Self-assembly concept, top view (above) and side view (below). A chip is presented at some distance away from the foil, and the magnetic field generated by pole pieces underneath the foil brings the chip in final position.

The chips need magnetisable features, so-called flux guides, to make them susceptible to the magnetic field. In the current design of the process, the magnetization of standard

Ni + Au bumps on the chip is used. The magnetic field is generated by pole pieces underneath the foil, which are connected through a yoke to a permanent magnet. During assembly, the foil is positioned with respect to a number of these alignment units, organized in an array structure which interspaces matches the interspacing of chips on the foil.

The die attach adhesive which is used to bond the chip to the foil serves as a fluidic cushion, offering chip mobility during the self-assembly operation. After chip presentation e.g. from a pick-up tool, the chip will be trapped by the magnetic field, land on the die attach adhesive, and will be attracted to the final position while floating on the adhesive. After reaching final position, the adhesive is cured. To geometrically constrain the die attach adhesive, a local hydrophilic area, considerably larger than the chip size ($\approx 4 \times 4 \text{ mm}$), is created by mask-based plasma treatment of the foil. A small volume ($\approx 1.0 \mu\text{l}$) of die attach adhesive is supplied to the hydrophilic area. Obviously, the viscosity of the die attach adhesive is of major importance for the cycle time of the operation. More details on the process and its physics can be found in [7].

The process has experimentally been researched using a laboratory set-up which consists of a magnet unit and a holder to position a PET foil with respect to the magnet unit. In the experiments, a chip is presented to the self-assembly field from a predefined starting location some distance above and away from the target location, and the trapping and alignment process is observed using camera systems. In the current experiments dummy chips were used (IZM41.1, $900 \times 900 \times 20 \mu\text{m}^3$, 4 IO, Ni+Au bond pads $\varnothing 250 \mu\text{m}$, 5-6 μm thickness).

Fig. 8 shows a typical alignment results. It was observed that immediately after release from the pick-up tool the chip starts to move in the direction of the target location. The chip aligns with respect to the maximum of the magnetic field gradient. With the low-viscosity adhesive currently used, the best achieved alignment cycle time at present is less than 1.0 sec (i.e. time elapsed between chip release from the pick-up-tool and reaching final position) and the precision is in the range of $\pm 100 \mu\text{m}$. More experimental results are reported on in [7].

Fig. 8. Typical result of an alignment experiment. A chip is presented by a pick-up-tool (left). There can be a considerable distance between the release point and the final position.

Adaptive interconnection

After the chip is placed on and bonded to the foil using the die attach adhesive, the interconnects have to be realised. In the Chip2Foil process this involves two steps: the position registration of the chip with respect to the circuitry on the foil in the chip area, and the creation of interconnects on an individual chip basis. The interconnection process essentially means that the end points of the foil circuitry need to be connected with the corresponding bond pads on the chip. This may be achieved in various ways. One option is to write conductive lines, e.g. by ink-jet printing or by laser-induced forward transfer (LIFT, [8]) approach. The advantage is that only conductive material is added where needed. However, both ink-jetting and LIFT do not meet the technical demands yet. LIFT is not yet mature enough for industrial implementation; equipment and tooling needed for successful commercial implementation of this process are not yet fully commercialized. Inkjet printing is a fairly well-established industrial process. However, the low thickness of deposited interconnect traces, which necessitates multi-pass printing to realize thicker traces and hence good electrical conductivity, is a significant disadvantage. In addition to that, inkjet-printed interconnects are prone to cracking at the edges of the chip due to the height difference between the bond pads and the foil circuitry. Hence, another approach to interconnection, which involves laser structuring of a screen printed conductive patch, was chosen in the Chp2Foil project. The process is shown in more detail in Fig. 9.

Fig 9. Interconnection approach: laser structuring of screen printed conductive patch.

First, the chip is encapsulated with a globtop material for final bonding and protection. Then, the chip position is measured with respect to alignment features around the chip area. The alignment features are added during the screen printing of the foil circuitry. Then, vias are laser drilled through the globtop to open up the chip bond pads. Next, in another screen printing operation a conductive silver patch is applied which fills up the vias and covers the glob-top layer including the endpoints of the foil circuitry. After curing of the patch, a laser scribing operation is used to structure the patch and divide it into mutually isolated conductive areas, creating electrical connections between the endpoints of foil circuitry and the bondpads on the chip.

A vision system is realised which has sufficient field of view (11x8.5 mm), resolution (pixel size in object plane 2.2 μm), depth of focus (150 μm) and low computation time

(allowing 50 chips/sec data processing). Fig. 10 shows the hardware and a result of an image analysis. This system identifies the locations of predefined features on the chip and on the foil and computes both the coordinates for the drilling of the globtop and the adaptive scribing paths required to connect each pad on the chip with its designated counterpart in the foil circuitry. Prior to the computation of the adaptive interconnection paths, another imaging step is required in order to identify the boundaries of the conductive paste applied to the region.

Fig 10. Vision system (left) and result of image analysis (right). Red/blue circles mark registration marks and chip pads identified by the system.

The selection of the laser source is directly related to the absorption spectra of the materials to be machined. As globtop material, Loctite 3730 (Henkel) was chosen. The material absorbs the Nd:YAG 266nm laser wavelength very well. This laser source allows fast machining. Also, the material is transparent for the wavelengths of light used in chip position image recognition. Fig. 11a shows a chip bondpad, exposed by via drilling through the globtop material.

Fig 11. Laser machining supported interconnection: (a) via machined through globtop material, exposing a chip bond pad, (b) laser structured silver patch on top of globtop material.

The screen printing application of the silver patch has shown to fill vias (diameters down to 80 μm), and makes reliable contacts with the Ni-Au bond pads on the chip. In current trials, a KrF-excimer laser with a wavelength of 248 nm was successfully used for scribing the patch because of its availability, see Fig. 11b, but for industrial implementation, again a Nd:YAG 266nm laser source is a suitable option to achieve high scribing speeds.

Reel-to-reel implementation

The technology required for the proposed UTC placement and interconnection process is currently researched and demonstrated in sheet-based research set-ups, and mostly for single chip processes only. In an industrial scenario, upscaling is required, and the eventual goal is to manufacture foil-based packages in a reel-to-reel (R2R) scenario. In an R2R scenario, the foil travels through the machine, possibly in a stop-and-go mode for some of the operations, and a 2D arrays of chips needs to be integrated. Throughput, i.e. the number of integrated chips per unit of time, and parallelisation are two of the main issues to be further investigated.

The major added value of the proposed concept is the ability to handle ultra-thin chips and place them on an adhesive layer, as obtained by the combination of non-contact presentation and self-assembly. In chip placement, a potential bottle-neck for throughput is the presentation process. If chips are presented using a manipulator, e.g. as in a die bonding machine, the machine travel time between wafer tape and assembly location may consume a substantial amount of the entire placement cycle time. Hence, in order to harvest the full potential of the approach and to increase throughput, parallelisation of chip presentation is essential.

Likewise, the interconnection process requires laser machining. In an industrial process it is possible to use a powerful laser source in combination with beam splitters and controllable optics to laser machine the interconnects of a number of chips in parallel with a single laser source. Parallelisation is feasible, but comes at the cost of a more complex optical system to control the laser beam. In addition, the image capturing and processing as well as the computation of laser tracks to be machined can be done very fast. However, the image capturing is single-chip oriented, and is defined by the position of the camera. In case of reel-to-reel production with an array of chips to be processed, it may be necessary to integrate multiple camera systems in the production line to meet throughput demands. This obviously adds to the machine cost.

Conclusions

A new total process for ultra-thin chip integration to polymer foils is described, combining self-assembly with an adaptive interconnection process. Individual chips as thin as 20 μm have successfully been released from wafer tape with cycle times as low as 50 msec. Chips were released some distance away from the target location, and the magnetic self-assembly force field has shown to be able to trap and align the chip on a die attach adhesive layer with a repeatability of approximately $\pm 100 \mu\text{m}$ in less than 1.0 sec alignment cycle time (current best values). For the magnetic trapping, the magnetisation of standard Ni + Au bumps on the chip was successfully exploited. To achieve acceptable alignment cycle times, a very low viscous adhesive is essential. To bring the chip in a unique in-plane orientation, the bondpad arrangement must be asymmetric. Adaptive interconnection on the basis of laser machining and structuring of a screen-printed conductive patch was successfully demonstrated for low IO-count chips.

Further work includes continued quantification and optimisation of the performance of each of the individual processes, in particular the self-assembly and the adaptive

interconnection process. Design rules which describe conditions for applying the process will be defined. Finally, a demonstrator communicative foil-based package for the Smart Blister application will be realised.

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