Experiments on 10Gb/s Fast Settling High Sensitivity Burst-Mode Receiver with On-Chip Auto-Reset for 10G-GPONs

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Abstract: This paper reports performance tests on a DC-coupled 10Gb/s burst-mode receiver with on-chip reset, designed for 10G-GPONs. Record short 2R settling time, high sensitivity and large loud/soft ratio is demonstrated in burst-mode operations at 2.5G/5G/10Gb/s.

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1. Introduction

A major challenge for next generation passive optical networks (PONs) is the realization of a set of 10Gb/s burst-mode physical medium dependent (BM-PMD) components, namely a burst-mode transmitter (BM-TX) at the subscriber optical network unit (ONU), and a burst-mode receiver (BM-RX) and burst-mode clock and data recovery (BM-CDR) at the optical line termination (OLT) of the PON system. Among these BM-PMD components, the 10Gb/s BM-RX is most challenging to design. It requires fast RX settling, to allow for a short burst preamble and hence high interactivity and throughput, combined with a high sensitivity and a wide dynamic range, to be compliant with installed optical distribution networks, or ODNs, and to support flexible network deployment. Recently both AC-coupled and DC-coupled BM-RXs have been reported for IEEE 802.3av 10G-EPONs [1][2], but these require 64B66B line coding and a relatively long RX settling time. Though FSAN has only endorsed XG-PON1 with asymmetrical 10/2.5 Gb/s transmission rates so far, a first symmetrical XG-PON with 10/10 Gb/s has been reported in [3]. The BM-RX reported in [3] is an AC-coupled design that still requires a total settling time of 360 ns including CDR. A DC-coupled design however can achieve a much shorter RX overhead at the physical layer [4]. This paper demonstrates the performance of a newly developed 10Gb/s APD-based BM-RX originally designed for symmetric 10G-GPON operation. It can process burst signals at 2.5G/5G/10Gb/s simultaneously without needing an external reset signal.

2. Realization of the 10Gb/s BM-RX

Fig. 1. The block diagram of the 10Gb/s DC-coupled BM-RX with on-chip auto-reset generation and activity detection.

Fig. 1 shows the block diagram of the 10Gb/s APD-based DC-coupled BM-RX. A burst-mode transimpedance-amplifier (BM-TIA) is DC-coupled with a burst-mode limiting-amplifier (BM-LA). The BM-TIA performs fast gain setting in three steps (High gain, Medium gain and Low gain) by means of a variable-gain TIA_c core followed by a variable-gain single-ended-to-differential (S2D) circuit. A dummy TIA_d generates the references for both the S2D

and the gain switch block. When a burst has ended, the BM-TIA is reset to high transimpedance gain for maximum RX sensitivity. When a new incoming burst exceeds a certain power threshold, the transimpedance switches to Medium gain, and is possibly further reduced to Low gain, all within a few nanoseconds, under the control of logic signal GS1 and GS2. Once set, the TIA transimpedance gain is locked and kept constant during the burst payload. Fig. 1 indicates that the BM-TIA has no reset pin. The reset signal is available in the subsequent BM-LA, and conveyed to the BM-TIA via common-mode signaling. The input stage of the BM-LA alters the common-mode voltage of the BM-TIA output. The BM-TIA extracts an on-chip reset signal out of these common mode changes.

The 10Gb/s BM-LA is a DC-coupled feedback-type RX. It implements a fast offset integrator with two switchable time constants as shown in Fig. 1. When a new burst arrives, the BM-LA first performs fast offset compensation and amplitude recovery with a short time constant. Once the correct threshold is established, the offset integrator switches to a larger time constant and enters a slow tracking mode, which is critical to provide a higher tolerance to consecutive identical digits (CIDs) within the payload. The DC-coupled fast response BM-LA needs a reset signal. In these experiments, the reset signal can be provided externally by the system, or generated internally by the BM-LA chip itself (auto-generated). In the latter case the BM-LA itself detects the end of a burst, resets the decision threshold to an initial state, and waits for the arrival of a next burst. As soon as new burst activity is detected on chip, it quickly enables the offset compensation loop to extract the decision threshold.

3. Integration of the 10Gb/s BM-PMD components and experimental results

New 10Gb/s BM-TIA and BM-LA components, recently fabricated in a 0.13 μm SiGe BiCMOS process, are integrated as shown in Fig. 2. To emulate the uplink PON system, two 1.3 μm burst-mode transmitters (BM-TXs) are alternately sending 10Gb/s bursts upstream. BM-TX1 is electro-absorption modulator laser (EML) based, it has an output power of +4.4 dBm and an extinction ratio (ER) of 10 dB. BM-TX2 is a DFB laser based TOSA, it has an output power of -0.8 dBm with an ER of 7 dB. The two TX outputs are combined by a 2x2 splitter, and fed to the BM-RX. The BM-RX is AC coupled to the BM-CDR board providing clock and data recovery.

Fig. 2. The 10Gb/s BM-PMD components for 10G-GPON upstream experiments.

We first evaluated the BM-RX on its own, with an external reset signal. The 10Gb/s burst packets consisted of a 76.8 ns preamble and a 1280 ns payload. The guard time between bursts was set to 25.6 ns. The payload was composed of a non-return-to-zero (NRZ) $2^{31}-1$ pseudo random bit sequence (PRBS) data pattern plus CID patterns with 72 bits of successive 1's resp. 0's. The APD multiplication factor M was set to 9. Fig. 3(a) shows the BER curves measured with an external reset signal. The measured input sensitivity of the BM-RX at a pre-FEC BER of 10^{-3} was -31.9 dBm for burst-mode back-to-back (BM-B2B). With 2 branches of BM-TXs, the BM-RX sensitivity measured on the weak packet emitted by BM-TX1 was -31.3 dBm for the worst case when the output power of BM-TX2 equals -6 dBm. The error-free input overload level was found to be higher than -5 dBm. This yields a dynamic range of more than 26.3 dB. The BM-RX was also assessed in different loud/soft ratios and the measured BM-RX penalties due to the preceding loud burst are shown in Fig. 3(b). The maximum BM penalty was only 0.6 dB at a loud/soft ratio of 25.3 dB.

Fig. 4(a) shows the measured BERs using the BM-RX with the BM-CDR. The preamble time was increased up to 150 ns to accommodate the CDR settling time. The input sensitivity at pre-FEC BER of 10^{-3} remains unchanged

when the BM-RX is followed by the BM-CDR. The BM-RX output thus provides already an almost ideal 2R-regenerated signal to the CDR.

Fig. 3. (a) The measured BER curves for BM-B2B and 2 TX branches; (b) BM penalty versus different load/soft ratio

Fig. 4. Measured BER curves (a) using BM-RX with BM-CDR; (b) at 2.5G/5G/10Gb/s in BM with and without an external reset signaling

We finally evaluated the BM-RX at different upstream data rates with on-chip auto-reset generation. In this experiment, the BM-TX2 operated at a data rate of 10Gb/s while the BM-TX1 was sending bursts at 2.5G, 5G and 10Gb/s respectively. For auto-reset and multiple-rate operation, the guard time and settling time were increased to 100 ns resp. 150 ns. The guard time up to 1 ms was also tested with on-chip auto-reset and the BM-RX works properly. The payload remains NRZ $2^{31}-1$ PRBS pattern plus CID patterns with 72 bits of 1's resp. 0's for different data rates. The measured BER curves are shown in Fig. 4(b). At 10Gb/s, the RX sensitivity penalty from using on-chip auto-reset generation instead of an external reset signal is limited to 0.3 dB at pre-FEC BER of 10^{-3} . For 2.5Gb/s operation we assume there is no strong FEC, and therefore the BER threshold was set to 10^{-10} . At this BER threshold the sensitivity penalty of using on-chip auto-reset is negligible for 2.5Gb/s operation. With auto-reset generation, an upward deviation of the BER curve is found when the input power is lower than -31 dBm. This is attributed to the fact that input signals less than -31 dBm are too weak for the on-chip auto-reset circuit in our current design, which targets supporting Class N2 optics defined for the XG-PON. This can be improved in a new design if needed.

Table 1: Performance summary of the DC-coupled BM-RX at 10Gb/s

10Gb/s Burst-mode	B2B (TX+RX)	BM-RX +CDR	BM-RX with 2 TX branches	BM-RX with external reset at 10G / 5G / 2.5Gb/s	BM-RX with on-chip auto-reset at 10G / 5G / 2.5Gb/s
Sensitivity (dBm)	-31.9	-31.9	-31.3	-31.3 / -32.7 / -33.0 @ 10^{-3}	-31.0 / -28.5 @ 10^{-10} / -28.9 @ 10^{-10}
Overload (dBm)	-5	-5	-6	-6	-6
Dynamic range (dB)	26.9	26.9	Load/soft 25.3	Load/soft 25.3 / 26.7 / 27.0	Load/soft 25.0 / 22.5 / 22.9

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6. References

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