PREFACE

The ACACES summer school wants to create an opportunity to learn new things and to meet new people. We believe that the 12 courses and the two invited talks – all by world class experts – suffice to reach the first goal.

The second goal is a bigger challenge. How can we bring the participants in contact with as many other participants of the summer school in one week? To reach this goal, we arranged to have all meals and coffee breaks together, there are long breaks, and very importantly – we organize a poster session on Wednesday afternoon.

The basic idea is that you can present your own research to the other participants, and that you learn more about the other participants’ research. We have put the poster session in the middle of the week so that people with a common research interest still have enough time during the rest of the week to discuss their mutual research interest, hopefully resulting in a long lasting research collaboration and joint research contributions. So, the poster session will help you in further developing your professional network, this is what HiPEAC is all about.

There will be 82 posters presented during the poster session. You will not have time to discuss them all during one afternoon. Therefore, we have collected the abstracts in a book of abstracts. The abstracts in this book were not reviewed as we did not want to exclude anybody from participating in the poster session, and from making new contacts. The sole purpose of the book is to prepare your visit to the poster session. You can in advance select the posters you want to discuss and then visit them (the order of posters on the posters panels is the same as in the book). If you present a poster yourself, make sure that you spend about 50% of your time at your poster, and the other 50% visiting other posters.

I wish you a very productive poster session

Koen De Bosschere
Summer School Organizer
# CONTENTS

Towards a Performance Scalable File System Design  
*Konstantinos Chasapis, Yannis Klonatos, Stelios Mavridis, Michail D. Flouris, Manolis Marazakis, Angelos Bilas*

Towards an HPC I/O framework for clusters of Virtual Machines  
*Anastassios Nanos, Nectarios Koziris*

A full custom modular switch for CMP Systems  
*Antoni Roca, José Flich, Federico Silla, José Duato*

A minimal/non-minimal routing algorithm for NoCs to misroute packets around congested areas  
*Masoumeh Ebrahimi, Masoud Daneshtalab, Pasi Liljeberg, Hannu Tenhunen*

An Approach to the Performance of Congestion Management Techniques in Interconnection Networks with Direct Topologies  
*Daniel Gomez-Garcia, Pedro Javier Garcia, Francisco José Quiles, Jesús Escudero-Sahuquillo, Juan Antonio Villar, José Flich, José Duato*

Exploring the Coherence Protocol Acceleration through the Interconnection Network  
*Lucía G. Menezo, Adrián Colaso, Valentín Puente, Jose-Ángel Gregorio*

Exploring the On-Board Interconnect Requirements of Multi-Chip Architectures  
*Karthikeyan Palavedu Saravanan, Alejandro Rico, Felipe Cabarcas, Alex Ramírez*

Exploring 3D-NoC based architectures  
*Daniele Bortolotti, Andrea Marongiu, Martino Ruggiero, Luca Benini*

A New Selection Policy for Low Power Networks on Chip  
*Diána Salemi, Maurizio Palesi*

DVFS Management in Real Processors  
*Vasileios Spiliopoulos, Georgios Keramidas, Stefanos Kaxiras, Konstantinos Efstathiou*

Online Performance Prediction in Processors with DVFS Capabilities  
*Qixiao Liu, Miquel Moreto, Jaume Abella, Francisco J. Cazorla*

Exploring the performance-energy tradeoffs in Sparse Matrix-Vector Multiplication  
*Vasileios Karakasis, Georgios Goumas, Nectarios Koziris*

Reducing energy consumption with flexible memory systems  
*Andreas Koltes, Robert Mullins*

Combining technologies to reduce energy in L1 data caches  
*Alejandro Valero, Julio Sahuquillo, Salvador Petit, Pedro López, José Duato*
Memory Hierarchy and Network Co-design through Trace-Driven Simulation
Mario Lodde, José Flich

Improving the World’s Fastest Cache Simulator
Andreas Sandberg, Peter Vestberg, Erik Hagersten

StatCC: Modeling Multi-Core Cache Sharing in a Fraction of a Second
David Eklov, David Black-Schaffer, Erik Hagersten

Using Miss Ratio Curves To Understand Program Optimization
Muneeb Khan, Nikos Nikoleris, Erik Hagersten

Towards Value-Aware Caches
Angelos Arelakis, Per Stenstrom

Cache Pirating: Measuring the Performance Impact of Cache Sharing
Nikos Nikoleris, David Eklov, David Black-Schaffer, Erik Hagersten

Scarphase: Fast Online Phase Classification
Andreas Sembrant, David Eklov, Erik Hagersten

How sensitive is processor customization to the workload’s input data sets?
Maximilien Breughe, Zheng Li, Yang Chen, Stijn Eyermans, Olivier Temam, Chengyong Wu, Lieven Eeckhout

Characterizing Phase Behavior for Dynamically Reconfigurable Architectures
Zhibin Yu, Nikola Puzovic, Antonio Portero, Roberto Giorgi

Communication Strategy for Embedded Distributed Architectures
Celine Azar, Stephane Chevobbe, Yves Lhuillier, Jean-Philippe Diguet

Coarse-Grained Reconfigurable Approach for Multi-Dataflow Systems
Nicola Carta, Francesca Palumbo, Luigi Raffo

Efficiently generating FPGA configurations through a stack machine
Fatma Abouelella, Karel Bruneel, Dirk Stroobandt

FPGAs for general purpose computing
Javier Olivito, Javier Resano

Peak Performance Model for a Custom Precision Floating-Point Dot Product on FPGAs
Manfred Muecke, Bernd Lesser, Wilfried N. Gansterer

Fast ASIP Design Space Exploration on FPGAs through Binary Translation
Sebastiano Pomata, Giuseppe Tuveri, Paolo Meloni, Menno Lindwer

Architectural Support for Concurrency on Reconfigurable Systems
Pavel Zaykov, Georgi Kuzmanov

A configurable and scalable multi-core architecture template supporting hybrid Model of Computation
Giuseppe Tuveri, Sebastiano Pomata, Simone Secchi, Paolo Meloni
Parallel Access Schemes for Polymorphic Register Files: Motivation Study
Catalin Ciobanu, Georgi Kuzmanov, Alex Ramirez, Georgi Gaydadgiev

Mapping irregular MPSoC topologies onto 2D-meshes
José Cano, José Flich, José Duato, Marcello Coppola, Riccardo Locatelli

Automated Architecture Synthesis and Application Mapping for ASIP based adaptable MPSoCs
Erkan Diken, Roel Jordans, Rosilde Corvino, Lech Joziwak, Menno Linduer

Thermal-aware SoC design through micro-architectures selective block replication
Dionisios Diamantopoulos, Kostas Stizlos, Sotiris Xydis, Dimitrios Soudris

Early Exploration of Partitioning Trade-offs for Heterogeneous MPSoCs
Prashant Agrawal, Robert Fasthuber, Praveen Raghavan, Tom Vander Aa, Francky Catthoor, Liesbet Van der Perre

Accelerating Embedded Systems with C-based Hardware Synthesis
Vito Giovanni Castellana, Christian Pilato, Fabrizio Ferrandi

Hardware OpenVG Rendering Engine
Yong-Luo Shen, Sang-woo Seo, Seok-Jae Kim, Hyun-Goo Lee, Hyeong-Cheol Oh

Automatic Run-time Parallelism Extraction for the Design of Hardware Accelerators
Silvia Lovergine, Christian Pilato, Fabrizio Ferrandi

Portability for Heterogeneous Parallel Architectures
Peter Calvert, Alan Mycroft

An Algorithm Template for Parallel Irregular Algorithms
Carlos H. González, Basilio B. Fraguela

Employing Helper Threads as a Parallelization Paradigm
Anastasios Katsigiannis, Nikos Anastopoulos, Konstantinos Nikas, Georgios Goumas, Nectarios Koziris

SCOOP: Source-level Compiler Optimizations for Parallelism
Foivos S. Zakkak, Dimitrios Chasapis, Polyvios Pratikakis, Angelos Bilas, Dimitris S. Nikolopoulos

SVP - a concurrency model for many-core computing
Q. Yang, C.R. Jesshope

A Predictive Modelling based Approach to Runtime Adaptation of Parallel Programs
Murali Krishna Emani, Michael O'Boyle

VMAD: a Virtual Machine for Advanced Dynamic Analysis
Alexandra Jimborean, Matthieu Herrmann, Philippe Clauss, Vincent Loechner

Elasticity through Fault-Tolerance in a Cloud-based Distributed Stream Processing Engine
Dimokritos Stamatakis, Kostas Magoutis
Improving efficiency in the data center - The case of data streaming applications
Shoaib Akram, Angelos Bilas
191

An Auto-tuning Solution to Data Streams Clustering in OpenCL
Jianbin Fang, Ana Lucia Varbanescu, Henk Sips
195

Rapid Prototyping in OpenCL with V-Parallel Process Networks
Ana Balevic, Bart Kienhuis
199

CUDA tuning and configuration parameters on Fermi architecture
Yuri Torres De La Sierra; Arturo Gonzalez Escribano; Diego R. Llanos Ferraris
203

Microscopic traffic simulation using CUDA
Pavol Korcek, Lukas Sekanina, Otto Fucik
207

Efficient Independent Component Analysis on a GPU
Rui Ramalho, Pedro Tomas, Leonel Sousa
211

GPU performance analysis using the FFT
Jacobo Lobeiras, Margarita Amor, Ramon Doallo
215

Memory-Hierarchy-Aware Decoding of Structured LDPC Codes on GPUs
Joao Andrade, Gabriel Falcao, Vitor Silva
219

Analysis of parallel sorting algorithms on different parallel platforms
Marko Misic, Milo Tomasevic
223

Optimally Mapping a CFD Application on a HPC Architecture
Ion Dan Mironescu, Lucian Vintan
227

Multi-layered Abstractions for Partial Differential Equations from High-level Descriptions
Florian Rathgeber, David A. Ham, Mike B. Giles, Paul H. J. Kelly, Graham R. Markall, Gihan R. Mudalige
231

Compiler analysis for improving OpenMP code generation
Sara Royuela, Roger Ferrer, Alex Duran, Xavier Martorell
233

Analysis and Visualization of Software
Pierre Caserta
237

Implementation and Empirical Comparison of Partitioning-based Multi-core Scheduling
Yi Zhang, Nan Guan, Wang Yi
239

Implications of Merging Phases on Scalability of Multi-core Architectures
Madhavan Manivannan, Ben Juurlink, Per Stenstrom
243

Architecture for a Million Core Processor
Zeus Gomez Marmolejo, Victor Garcia, Alex Ramirez, Nacho Navarro
245

Exploiting Scalability on the Intel SCC Processor
Andreas Diavastos, Panayiotis Petrides, Gabriel Falcao, Pedro Trancoso
253
MapReduce for the Single-Chip-Cloud Architecture
Anastasios Papagiannis, Dimitrios S. Nikolopoulos

Memory-intensive parallel computing on the Single Chip Cloud Computer: A case study with Mergesort
Nicolas Melot, Kenan Avdic, Christoph Kessler, Jörg Keller

Graphic Rendering Application Profiling on a Shared Memory MPSoC Architecture
Matthieu Texier, Raphael David, Karim Ben Chehida, Olivier Sentieys

Pipelining Producer-Consumer Tasks using Custom Multi-Core Architectures
Ali Azarian, Joao M. P. Cardoso

User-directed Auto-vectorization in OmpSs
Diego Caballero, Xavi Martorell, Roger Ferrer, Alex Duran y Eduard Aigüadé

T-Star (T*): An x86-64 ISA Extension to support thread execution on many cores
Antoni Portero, Zhibin Yu, Rania Mameesh, Roberto Giorgi

PEPPHER: Performance Portability and Programmability for Heterogeneous Many-core Architectures
Siegfried Benkner, Sabri Pllana, Jesper Larsson Träff, Philippas Tsigas, Andrew Richards, Raymond Namyst, Beverly Bachmayer, Christoph Keßler, David Moloney, Peter Sanders

Facing the Challenges of Heterogeneous Systems at Application Runtime
Mario Kicherer, Wolfgang Karl

Fast JIT Code Generation for x86-64 with LLVM
Viktor PAVLU, Andreas KRALL

Hardware Support for Dynamic Languages
Pascal Schleuniger, Sven Karlsson, Christian W. Probst

NumCIL: Numeric operations in the Common Intermediate Language
Kenneth Skovhede

Emeraude: Embedded Real-Time Adaptative Virtualization for Post-Moore Architectures
Pierre Boulet, Julien Forget, Abdoulaye Gamatié, Laure Gornord, Samuel Hym, Richard Olejnik

How to model real-time task constraints on a high-performance processor simulator
José Luís March, Julio Sahuquillo, Salvador Petit, Houcine Hassan, José Duato

A Count-Based Scheme for Fault Detection in Memory Arrays
Yiannakis Sazeides, Bushra Ahsan, Isidoros Sideris, Lorena Ndreu, Sachin Idgunji, Emre Ozer

Cryptography on embedded devices with application to in-vehicle communication
Pal-Stefan Murvay