

FPGA implementation of online finite-set model based predictive control for power electronics

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Abstract—Recently there has been an increase in the use of model based predictive control (MBPC) for power-electronic converters. MBPC allows fast and accurate control of multiple controlled variables for hybrid systems such as a power electronic converter and its load. The computational burden for this control scheme however is very high and often restrictive for a good implementation. This means that a suitable technology and design approach should be used.

In this paper the implementation of finite-set MBPC (FS-MBPC) in field-programmable gate arrays (FPGAs) is discussed. The control is fully implemented in programmable digital logic by using a high-level design tool. This allows to obtain very good performances (both in control quality, speed and hardware utilization) and have a flexible, modular control configuration. The feasibility and performance of the FPGA implementation of FS-MBPC is discussed in this paper for a 4-level flying-capacitor converter (FCC). This is an interesting application as FS-MBPC allows the simultaneous control of the output current and the capacitor voltages, yet the high number of possible switch states results in a high computational load. The good performance is obtained by exploiting the FPGA's strong points: parallelism and pipe-lining. In the application discussed in this paper the parallel processing for the three converter phases and a fully pipelined calculation of the prediction stage allow to realize an area-time efficient implementation.

Index Terms—MBPC, predictive control, FPGA implementation, flying-capacitor inverters, programmable digital hardware

I. INTRODUCTION

Multilevel converters were developed to meet a growing need for higher power converters as the series connection of switches allows a higher voltage handling. Furthermore, these topologies can apply intermediate voltage levels resulting in an output voltage with lower harmonic distortion. Due to several advantages over other multilevel topologies, flying capacitor (FC) converters have attracted a lot of interest, [1], [2]. The capacitor voltages of the FC converter need to be regulated. This can be achieved either passively by using natural balancing, or actively by measuring and controlling the capacitor voltages. There is a great interest in the active control as the passive control fails in certain circumstances, [2]. This flying capacitor voltage control needs to be implemented together with the inverter output current control.

The simultaneous control of the FC inverter output current and flying capacitor voltages is done preferably with a true multivariable control. Model based predictive control (MBPC) is particularly capable of controlling multivariable systems.

Furthermore it is very well suited to control systems with inherently discrete control signals. For power electronic converters the number of switch states is indeed limited to a finite set. As these finite-set model based predictive controllers are an interesting option their application in power converters has increased tremendously [1]–[4].

This increase was enabled by the availability of high processing power. However the largest drawback of the MBPC algorithm remains the large computational burden, especially for an on-line implementation of FS-MBPC where the calculations need to be done in real-time. This is often stated as the most impeding factor for the wide-spread adoption of MBPC in power electronics. As such there is a large interest in techniques to reduce this computational burden and indeed several design choices have to be made when implementing MBPC. However, these choices can influence the control quality and care has to be taken to avoid a significant deterioration in control quality as a result of a reduction in computational burden. A method based on the calculation of the mean square error (MSE) of the controlled variables is discussed in [4] to evaluate the impact of design choices on the control quality. In [4] the MSE-analysis was used to establish a good range of cost function weight factors. With the same analysis the model simplification proposed in [1] was shown to be unacceptable.

Furthermore it was shown in [4], [5] that the algorithm without model simplification was very feasible to implement. Although many authors report difficulties with the online implementation of the large number of calculations needed for MBPC within the short cycle times needed in power electronics, the limitations often arise due to the choice of the technology for the implementation and the design approach that is used.

In this paper the feasibility to implement FS-MBPC for power electronics and the advantages for an FPGA implementation are addressed. As a design example a 4-level flying-capacitor converter is chosen, which is controlled very satisfactorily with both resources and calculation time to spare at an update frequency of 20 kHz. To this end the converter topology and finite-set model based predictive control are discussed in section II. Section III discusses different design choices and their impact on the computational load. The actual design objectives together with the design approach and FPGA utilization are discussed in section IV. Finally experimental results are shown to attest to the high control quality.

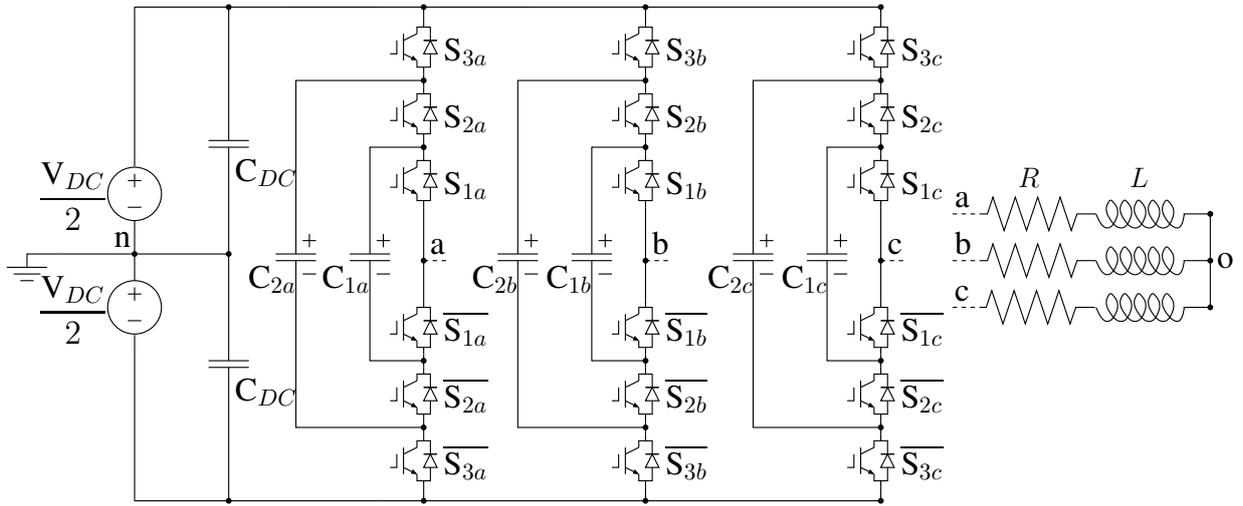


Figure 1: 4-level flying capacitor converter topology.

#	S_{1x}	S_{2x}	S_{3x}	V_{xn}
1	0	0	0	$-V_{DC}/2$
2	1	0	0	$-V_{DC}/6$
3	0	1	0	$-V_{DC}/6$
4	0	0	1	$-V_{DC}/6$
5	1	1	0	$V_{DC}/6$
6	0	1	1	$V_{DC}/6$
7	1	0	1	$V_{DC}/6$
8	1	1	1	$V_{DC}/2$

Table I: Switch states and the corresponding output voltage (when $V_{C_{1x}} = V_{DC}/3$ and $V_{C_{2x}} = 2V_{DC}/3$)

II. MBPC FOR FC INVERTERS

A. Flying capacitor inverter topology

The topology of a three-phase, four-level FC converter is depicted in figure 1. It uses 3 pairs of complementary controlled switches, $(S_{ix}, \overline{S_{ix}})$ with $i = 1, 2, 3$ per phase x , where $x = a, b, c$. These switches make it possible to connect the flying capacitors C_{1x} and C_{2x} in series with the load (an RL series connection). The series connection of the flying capacitor produces an intermediate output voltage. An overview of the possible switch states and their resulting output voltage is given in table I. If the upper switch of the switch pair i is closed, S_{ix} is 1, otherwise S_{ix} is zero. When the flying capacitor is connected in series with the load, the voltage of the capacitor changes as the load current flows through the capacitor. The voltages of the flying capacitors C_{1x} and C_{2x} in a four-level converter should always be kept at $\frac{V_{DC}}{3}$ and $\frac{2V_{DC}}{3}$ respectively. This choice provides optimal voltage rating of the switches as this only has to be $\frac{V_{DC}}{3}$. Of the 8 switch states for each phase, 6 switch states produce the 2 intermediate output voltages (3 redundant states per intermediate level). This makes it possible to perform a correction of the capacitor voltage for both current directions and thus control the capacitor voltage.

B. FS-MBPC algorithm

The principles of MBPC are explained and applied to the current control of multilevel converters in this section. In this paper a discrete-time controller operating with a fixed update frequency is considered. The two main control objectives for MBPC with multilevel converters are the tracking of the reference current and the balancing of the flying capacitor voltages which is done simultaneously by the multivariable control scheme. To this end the inputs for the FS-MBPC algorithm are the reference values and the measurements of phase currents and flying capacitor voltages. The output of the algorithm is one of the possible switch states of the converter, without using any modulation scheme. At every update instant a new switch state can be applied and is maintained during the entire update period. This results in a spread spectrum switching frequency. The average switching frequency per switch will certainly be lower than the update frequency, f_u .

MBPC is a strategy to control selected state variables by an optimization of the future switch states. For the optimization the future state variables need to be calculated for all possible future switch state sequences. Three steps can be defined: estimation, prediction and optimization step.

In the estimation step the state variables are calculated at the end of the current update period using the switch state which is currently applied.

The next step, the prediction step, covers future update periods where all possible future switch state sequences are considered. The number of update periods considered in the prediction step is denoted by N , the prediction horizon.

In the optimization step the most appropriate switch state sequence is selected, of which the first switch state is applied at the next update instant. At that update instant a new measurement sample starts a new iteration of the MBPC.

Estimation

At update instant k , the measurements of the phase currents

\mathbf{i}_x^k with $x = a, b, c$ and the flying capacitor voltages \mathbf{v}_{c1x}^k and \mathbf{v}_{c2x}^k are obtained (throughout this paper bold variables denote measurements and superscript k denotes the k th update period). At the end of this update period the currents and voltages will have changed due to the inverter switch state applied. This change is estimated based on the measurements, the applied switch state \mathbf{S}_{ix}^k and the model.

The switch state \mathbf{S}_{ix}^k of the converter does not change during the update period and it is assumed that the possible change in capacitor voltage is small and slow enough to be neglected when calculating the output voltage. Under these assumptions the following expressions for the load voltage v_{xo} are obtained from the converter output voltages v_{xn} and the star-point voltage v_{on} :

$$v_{xn}^{k+1} = \left(\mathbf{S}_{3x}^k - \frac{1}{2} \right) V_{DC} - (\mathbf{S}_{3x}^k - \mathbf{S}_{2x}^k) \mathbf{v}_{c2x}^k - (\mathbf{S}_{2x}^k - \mathbf{S}_{1x}^k) \mathbf{v}_{c1x}^k \quad (1)$$

$$v_{on}^{k+1} = \frac{v_{an}^{k+1} + v_{bn}^{k+1} + v_{cn}^{k+1}}{3} \quad (2)$$

$$v_{xo}^{k+1} = v_{xn}^{k+1} + v_{on}^{k+1} \quad (3)$$

The output currents at $k+1$ have to be estimated as well. The expression for the current at $k+1$ consists of the free response and forced response (i.e. because of the applied voltage):

$$i_x^{k+1} = e^{-\Delta \frac{R}{L}} i_x^k + \frac{1 - e^{-\Delta \frac{R}{L}}}{R} v_{xo}^{k+1} \quad (4)$$

In equation (4) R and L are the resistive and inductive parts of the load respectively and $\Delta = \frac{1}{f_u}$ is the update period.

Although the influence of the variation of v_{c1x} and v_{c2x} on the output voltage and currents is neglected, the flying capacitor voltages at update instant $k+1$ have to be estimated. The switch state defines if the load current passes through the capacitors and in which sense, expressed by $(S_{2x}^k - S_{1x}^k)$ in (5) and $(S_{3x}^k - S_{2x}^k)$ in (6). The voltage variation of the flying capacitors, with capacitance values C_1 and C_2 , depends on the average current in an update period:

$$v_{c1x}^{k+1} = v_{c1x}^k + \frac{\Delta}{C_1} \frac{\mathbf{i}_x^k + i_x^{k+1}}{2} (S_{2x}^k - S_{1x}^k), \quad (5)$$

$$v_{c2x}^{k+1} = v_{c2x}^k + \frac{\Delta}{C_2} \frac{\mathbf{i}_x^k + i_x^{k+1}}{2} (S_{3x}^k - S_{2x}^k) \quad (6)$$

Prediction

From update instant $k+1$, the controller can use any possible output during each update period to bring the controlled variables closer to their desired values. The controller thus predicts the outcome of all possible switch states over the entire prediction horizon, from $k+1$ to $k+1+N$, based on the estimations at $k+1$.

In the prediction step the same system model as in the estimation step is used. One important difference is that the output current and flying capacitor voltage at update instant $k+i$ for $i \in [1, N]$ of course can not be measured. As such the estimated (for $i=1$) or predicted values (for $i \in [2, N]$) from the previous steps are used. This results in the following set of

equations to evaluate for all possible switch states sequences, for $i \in [1, N]$:

$$v_{xn}^{k+i+1} = \left(S_{3x}^{k+i} - \frac{1}{2} \right) V_{DC} - (S_{3x}^{k+i} - S_{2x}^{k+i}) v_{c2x}^{k+i} - (S_{2x}^{k+i} - S_{1x}^{k+i}) v_{c1x}^{k+i} \quad (7)$$

$$v_{on}^{k+i+1} = \frac{v_{an}^{k+i+1} + v_{bn}^{k+i+1} + v_{cn}^{k+i+1}}{3} \quad (8)$$

$$v_{xo}^{k+i+1} = v_{xn}^{k+i+1} + v_{on}^{k+i+1} \quad (9)$$

$$i_x^{k+i+1} = e^{-\Delta \frac{R}{L}} i_x^{k+i} + \frac{1 - e^{-\Delta \frac{R}{L}}}{R} v_{xo}^{k+i+1} \quad (10)$$

$$v_{c1x}^{k+i+1} = v_{c1x}^{k+i} + \frac{\Delta}{C_1} \frac{i_x^{k+i} + i_x^{k+i+1}}{2} (S_{2x}^{k+i} - S_{1x}^{k+i}) \quad (11)$$

$$v_{c2x}^{k+i+1} = v_{c2x}^{k+i} + \frac{\Delta}{C_2} \frac{i_x^{k+i} + i_x^{k+i+1}}{2} (S_{3x}^{k+i} - S_{2x}^{k+i}) \quad (12)$$

Optimization

Once the trajectories of the state variables for all possible control sequences have been calculated, the optimal sequence can be selected by evaluation of a cost function g^k . The sequence resulting in the minimal cost is then selected and the first switch state is applied by the controller at time instant $k+1$. At this time $k+1$, the algorithm is started again, resulting in a so-called receding horizon.

The cost function assigns a cost to a deviation of the state variables from their desired values. When using a quadratic cost function the converter phase cost function g_x^k has a form as defined in equation (13):

$$g_x^k = W_{k+2} g_x^{k+2|k} + \dots + W_{k+N+1} g_x^{k+N+1|k}, \quad (13)$$

where the partial cost functions $g_x^{j|k}$ for $j \in [k+2, k+N+1]$ are given by:

$$g_x^{j|k} = (i_{x,r}^j - i_x^j)^2 + W_{v_{c1}} (v_{c1,r}^j - v_{c2x}^j)^2 + W_{v_{c2}} (v_{c2,r}^j - v_{c2x}^j)^2. \quad (14)$$

The weight factor W_{k+i+1} , $i \in [1, N]$, expresses the relative importance of the error in update period $k+i+1$. The weight factors $W_{v_{c1}}$ and $W_{v_{c2}}$ express the relative importance of errors in the flying capacitor voltages compared to an error in the output current. The cost of these errors is defined with respect to the respective reference values where $i_{x,r}$, $v_{c1,r}$ and $v_{c2,r}$ are the reference values for the phase current, the voltage of capacitor C_1 and the voltage of capacitor C_2 respectively. When $N=1$, the resulting converter phase cost function is:

$$g_x^k = (i_{x,r}^{k+2} - i_x^{k+2})^2 + W_{v_{c1}} (v_{c1,r}^{k+2} - v_{c2x}^{k+2})^2 + W_{v_{c2}} (v_{c2,r}^{k+2} - v_{c2x}^{k+2})^2 \quad (15)$$

The best switching action is found by minimising the total cost function g^k , which is the sum of all g_x^k :

$$g^k = g_a^k + g_b^k + g_c^k. \quad (16)$$

III. CHOICE OF DESIGN PARAMETERS

A. Design parameters to choose

Clearly the FS-MBPC algorithm has several design parameters that need to be chosen carefully to achieve a satisfactory and implementable control. Very important design parameters in terms of overall control quality are the weight factors for the relative capacitor voltage tracking error, $W_{v_{c1}}$ and $W_{v_{c2}}$. Although these parameters are very important, their influence will not be discussed here as they have little or no impact on the implementation (the only small impact is the size of the fixed point data types that need to be used in the calculations). A thorough discussion on the selection of these weight factors is given for a 3-level inverter in [4], and for a 4-level inverter in [6]. In [4], [6] furthermore the value of the mean squared error of the output current and capacitor voltages is shown to be a good measure to evaluate the overall control quality and to analyse the influence of certain design choices.

During the implementation of the MBPC, the designer can also choose to reduce the model complexity and as such reduce the computational burden. One particular model simplification is proposed in [1], where the interaction of the three phases through the star-point equations is neglected. In the system model it is clear from equations (8)-(9) that the load phase voltage is indeed determined by the phase output voltages of all phases and as such a coupled set of equations should be solved. In [4], [6] it has been shown that this model simplification is not acceptable as it reduces the control quality significantly and as such it will not be considered here.

A reduction of the number of equations to solve can be obtained by imposing restrictions on the allowed switch state transitions. These restrictions can also be imposed to improve the output voltage quality of the inverter, which is discussed in [7]. The implications for the computational demands for the resulting restricted finite set of allowed switch states is discussed here.

Of course the extent of the prediction horizon, N , is also a very important design choice for FS-MBPC. As discussed further on, increasing the prediction horizon quickly increases the number of calculations. However in [4], [6] it has been shown that this does not increase the control quality if no additional control terms are added in the cost function (such as number of switch events).

B. Computational demands

The model (equations (7)-(12)) of the flying capacitor converter (FCC) shows that the equations are fully coupled and for an m -phase, n -level converter $2^{m(n-1)}$ switch combinations have to be evaluated in the prediction step. In this case of a 3-phase, 4-level inverter that means 512 switch combinations per update period in the prediction step.

In table II, the number of switch states to evaluate is shown for a 4-level inverter for a prediction horizon of $N = 1$ and $N = 2$ and for different restrictions on the allowed switch state transitions. As can be seen in table II the number of switch states for unrestricted switch transitions is already

Table II: Number of switch state combinations to evaluate in the prediction step for FS-MBPC of 4-level FCC

N	restrictions	
1	single-switch	64
1	next-level	343
1	no	512
2	update 1 = single-switch update 2 = single-switch	4096
2	update 1 = next-level update 2 = single-switch	21952
2	update 1 = next-level update 2 = next-level	117649
2	no	262144

considerable for $N = 1$ with 512 switch states to evaluate, but very high for $N = 2$. However some restrictions can be applied. A first restriction that can be applied is 'next-level' switching, where each inverter phase can only change from a certain voltage level to an adjacent level or remain in the same voltage level. For example the output voltage level can change from $\frac{-V_{DC}}{6}$ to $\frac{V_{DC}}{6}$ or $\frac{-V_{DC}}{2}$ or remain at $\frac{-V_{DC}}{6}$, but can not change to $\frac{V_{DC}}{2}$. This is a very mild restriction and at each update instant the inverter switch state can toggle between redundant states to balance the capacitors directly. With either 4 (for $\frac{V_{DC}}{2}$ and $\frac{-V_{DC}}{2}$) or 7 possible switch state transitions (for the intermediate levels) a maximum number of 343 switch state changes are possible and have to be evaluated per update instant. A second restriction that can be applied is 'single-switch' switching, where for each inverter phase only one of the three switch pairs can change state. This restricts the number of changes per phase to 4 and thus 64 switch states have to be evaluated. With these restrictions the capacitors can not be balanced while keeping the same intermediate output voltage level. As can be seen in table II the restrictions allow to reduce the number of switch state combinations that need to be evaluated for $N = 2$. This shows that a choice of the design parameters strongly influences the computational burden. However the implications on the control quality for these restricted methods have to be evaluated with the MSE-method proposed in [4], [6]. For the unrestricted horizon expansion to $N = 2$ it has been shown [4], [6] that it is only sensible if other control objectives are added in the cost function. As such the remainder of the paper will focus on a prediction horizon of $N = 1$ with unrestricted switching.

In that case 512 switch combinations have to be evaluated in the prediction phase. The prediction phase consists of the evaluation of the equations (7)-(12). In table III the number of calculations per switch combination evaluation (prediction and cost function) is shown, the operations are also listed by type. Clearly the execution of the prediction and optimization stage is a large computational burden. The last line of table III gives the total number of operations to be executed during the prediction and optimization phase.

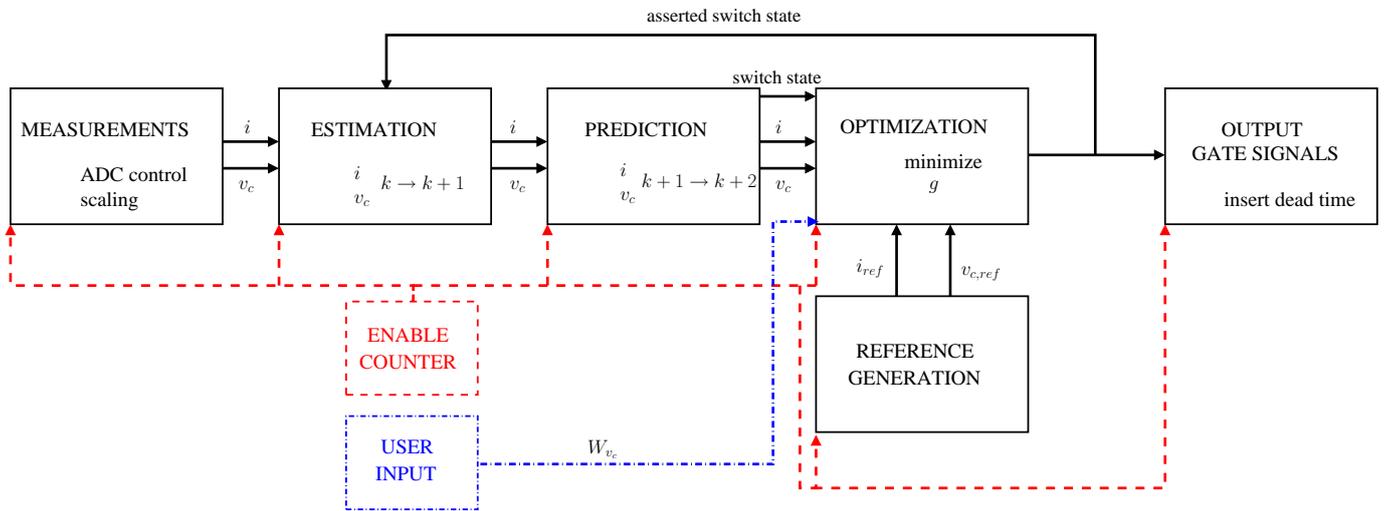


Figure 2: Block scheme of FS-MBPC with the constituting functions

Table III: Number of operations for FS-MBPC of 4-level FCC in the prediction and optimization step for each switch state possibility (prediction horizon $N = 1$)

addition	16
subtraction	24
constant mult.	14
multiplication	11
total per switch state	65
total all switch states	33280

The large number of calculations to perform clearly can be prohibitive for an implementation with reasonable update period on microcontrollers or DSPs, but with a proper design methodology it is very feasible on FPGA as discussed in the following section.

IV. FPGA IMPLEMENTATION

A. Design objectives and concept

During the implementation process of MBPC for FCCs in the FPGA the aim is on the following goals:

- **Obtained speed:** to achieve an acceptable control quality, high update frequencies (short algorithm cycle times) are required. Here we use a 20 kHz update frequency ($50\mu s$ cycle time).
- **Used resources:** in FPGAs the speed can be increased by paralleling processes, however the required resources (FPGA slices, multipliers) have to be available.
- **Reusability:** a proper modular design allows for the reuse and straightforward adaptation of function blocks when increasing the number of levels or the prediction horizon.
- **High-level configuration:** to easily and quickly configure different versions for research.

The high-level configuration was done with the System Generator toolbox for Simulink/Matlab from Xilinx. It provides an

environment to graphically build up the desired functionality in Simulink and to generate the FPGA bitstream, but allows also for the inclusion of low level VHDL code (e.g. for ADC-communication over SPI). Furthermore a modular build-up of the configuration comes naturally in this environment. In the FPGA implementation the operations are grouped in: estimation, prediction and optimization. This is shown in figure 2, where the entire block diagram is given. The other blocks are: measurements (for the ADC communication and scaling), reference generation (sinusoidal current reference and setpoint for capacitor voltages) and output (switch signal update and switch dead-time).

Within each block signal latency is provided for correct timing of the operations. Each block is enabled separately, based on a central counter, as such the blocks are decoupled and reusable in other designs. This modular design makes the implementation very scalable to higher level FCCs.

As mentioned before the prediction and optimization blocks present the largest computational burden. As such these blocks form the main core of the implementation and need to be well designed, keeping calculation time and resources in check. This is done by exploiting the FPGA advantages. To improve speed the calculations are done in parallel for the three phases. Also the calculations for the cost function terms are done in parallel. The total latency to perform the calculations in the prediction phase in our design is 21 clock cycles. However, it will not be possible, nor desirable, to parallel the calculations for all switch combinations due to the limited FPGA resources. Thus, to find a good balance between speed and resources, the prediction block needs to calculate the results for all switch combinations sequentially. With a calculation time of 21 clock cycles per switch combination, the total calculation time for the evaluation of the 512 switch combinations would amount to 10752 clock cycles. This makes short cycle times impossible. For all switch combinations however the same equations need to be evaluated. With the proper timing this

allows of the prediction block is provided, for a pipelined execution of the evaluation of all switch combinations. During the start-up phase of the pipeline no results are available at the output yet but a new switch state is fed into the pipeline at each clock cycle. During the steady-state of the pipeline a new switch state is fed into the pipeline and the results of the switch state loaded 21 clock cycles earlier becomes available at the output, for each clock cycle. During the last phase no new switch states are fed into the pipeline but a new result is still produced until the pipeline is 'empty'. With this fully pipelined prediction block all prediction equations take only $512+21=533$ clock cycles. The optimization block is also fully pipelined and has a calculation latency of 2 clock cycles. This means that all prediction and optimization calculations are performed in 535 clock cycles. Due to the fully pipelined design, scaling the prediction block to higher levels is easily done by duplicating the calculations for the flying capacitor and increasing the counter generating the switch combinations.

B. Design results: time and resource utilization

The FC converter is controlled with an Xilinx VirtexII-Pro FPGA (XUPV2P-30), clocked at 100 MHz. With a clock frequency of 100 MHz and an update period of 20 kHz there are 5000 clock cycles per update period. Figure 3 shows the timing diagram for the implemented 4-level FCC FS-MBPC. The independent enabling can be seen. The values for the time intervals are given in table 3. The time needed for the measurements and reference generation t_{m+r} is $5 \mu\text{s}$, although the ADCs allow a reduction to $1 \mu\text{s}$.

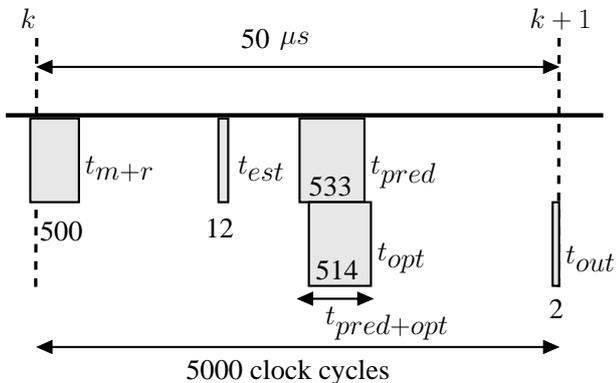


Figure 3: Timing of 4-level FCC MBPC

The time needed for the estimation t_{est} and output generation t_{out} is very small. Clearly the prediction and optimization phases use the most time. Note however that in this design the estimation and prediction phases use comparable amounts of resources, however the reuse of the prediction core to implement the estimation step is a very feasible and straightforward step to reduce the resource utilization. The time needed to calculate all 512 possible results t_{pred} and their cost function t_{opt} is only 535 clock cycles ($5.35 \mu\text{s}$), thus achieving about 6220 million operations per second (MOPS) for the prediction core. Clearly the obtained speed is more than sufficient: only

Table IV: Timing for the 4-level FCC MBPC

	clk cycles	time (μs)	% cycle time
t_{m+r}	500	5.00	10.00%
t_{est}	12	0.12	0.24%
$t_{pred+opt}$	535	5.35	10.70%
t_{out}	2	0.02	0.04%
total	1049	10.49	20.98%

Table V: FPGA utilization for the 4-level FCC MBPC

	used/available	% used
Slices	5952/13696	43%
18x18 mults	38/136	27%
PowerPC	0/2	0%

21% of the cycle time is actually needed. This is mainly due to the parallel, pipelined prediction and optimization stage.

In table V the used resources of the XUPV2P-30 are given. Only a fraction of the available resources are used. Even much cheaper FPGAs, such as the Spartan-3E-1200, can be used to implement this control. Further improvement in the resource usage are possible with the further optimization by using the same hardware for estimation and prediction steps. Also System Generator allows to trade off between slices and multipliers if needed to fit a design in a particular FPGA. The spare cycle time and resources create a number of possible options for implementations with a higher level FCC or larger prediction horizon by using this design with the parallel and pipelined prediction core.

V. EXPERIMENTAL RESULTS

The setup is a four-level flying capacitor converter constructed from in-house, half-bridge power electronic building blocks (PEBBs) as discussed in [8]. Each phase is equipped with a LEM LTS-25-NP current sensor to measure the output current. The appropriate signal conditioning and a 12bit ADC (National Semiconductor ADCS7476MSPS) provide a digitization on the PEBB. The flying capacitor voltages are measured in each phase leg with an instrumentation amplifier circuit and also digitized on the PEBB. The measured output currents and flying capacitor voltages are digitally transmitted to the FPGA, as such high resolution measurements are obtained. In the design of (FC) converters for model predictive control schemes the measurement quality is very important as it directly influences the obtained control quality.

In figure 4 a measurement is shown for the coupled control for the 4-level FCC. The output current reference is a 50Hz sine with 2A peak value and the flying capacitor voltage references are chosen according to a classical 3:2:1 ratio to the bus voltage V_{DC} . Clearly both the current and FC voltages are controlled close to their references. As the weight factor $W_{vc1} = 10$ is larger than the weight factor $W_{vc2} = 2.16$, v_{c1} stays closer to its reference than v_{c2} .

VI. CONCLUSIONS

In this paper an FPGA implementation for the online finite-set model based predictive control of flying-capacitor converters is discussed. Attention is paid to achieve high efficiency in time and resource utilization. By paralleling parts of the calculations and fully pipelining the prediction and optimization stages a design is obtained that is straightforward to scale to other numbers of levels or prediction horizons. The obtained control quality is very satisfactory. The design clearly showcases the calculation power of FPGAs and their application potential as the most interesting technology to implement online FS-MBPC for power electronics.

ACKNOWLEDGEMENT

This work was supported by the Research Foundation Flanders (FWO) under Project G.0665.06 and by the Interuniversity Attraction Pole under Project (IUAP) P6/21. The work of T.J. Vyncke was supported by a Ph.D. fellowship from the Research Foundation Flanders (FWO).

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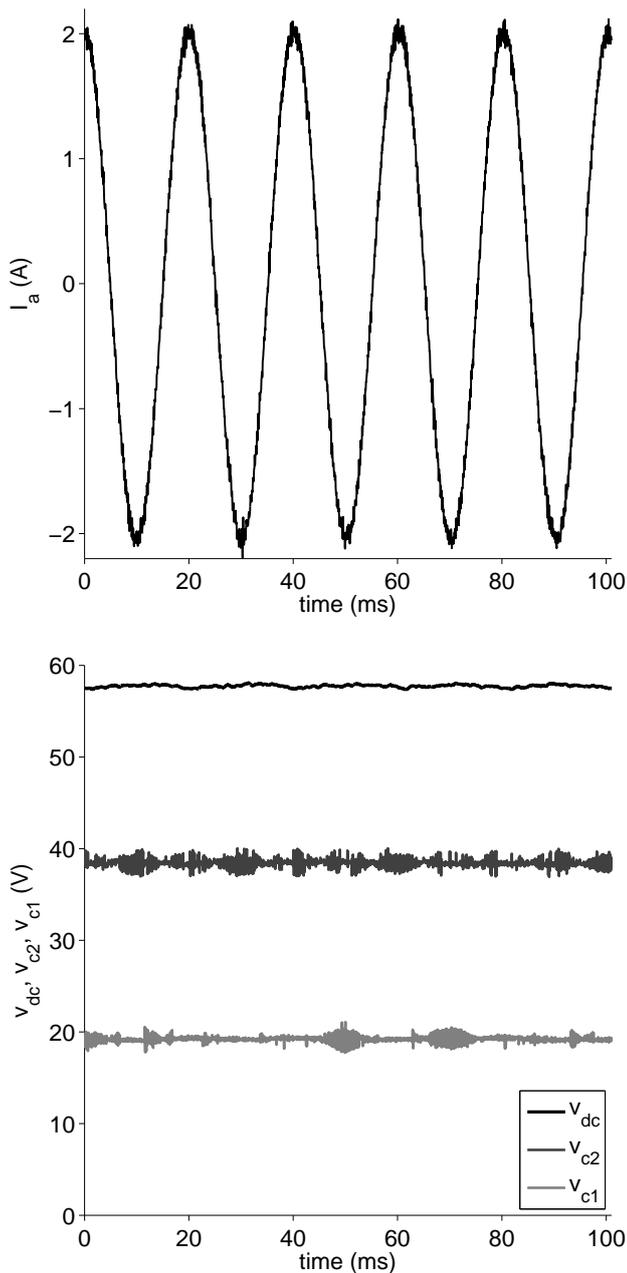


Figure 4: Measurement of output current (top) and flying capacitor voltages (bottom) of one phase for 4-level FCC