Foundry processes for silicon photonics

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ECIO
ePIXfab

### Prototyping

- Multi project wafer access to silicon photonic technologies
  - share mask and process costs
  - imec and LETI technologies
  - for R&D/pre-commercial use

### Training

- Basic training on ePIXfab technologies, design, and MPW operation

### Supply chain

- Access to supply chain:
  - design automation
  - packaging
  - manufacturing
Outline

• Passive device technology & considerations
• Active device considerations
• Wafer testing
• Design
• Prototyping access
Acknowledgement

• Si photonics platform team Ghent Univ. & imec
  • Wim Bogaerts, Philippe Absil, Peter Verheyen, Hui Yu, Adil Masood, Shankar Selvaraja, Jin Guo, Pieter Dumon

• The photonics research group
PROCESS TECHNOLOGY
Options

• Integration in existing CMOS process
  • Today
  • Foundry MPW & manufacturing
  • Not built for photonics
  • May need some adaptations
  • Example:
    • Luxtera/Freescale

• Custom process in your own fab
  • Freedom
  • €€€€€€€€€€
  • Example: Kotura
Options

• Semi-custom processes in standard fab
  • Today in MPW and LVM
  • Technology & PDK development by fab
  • Dedicated processes, transferable to foundry
  • Flexibility
  • Re-use as much as possible
• Examples:
  • imec
  • LETI
imec technology: waveguides

Etched wire in silicon

- 450 x 220 nm$^2$
- straight loss: 1.84 dB/cm
- bend losses $\sim$ 0.01 dB/90° (3 µm radius)

Transmission [dB] vs. spiral length [cm]

-1.84 (±0.1) dB/cm
Waveguide module

1. SOI wafer
2. Bottom Antireflective coating (BARC)
3. BARC bake
4. Resist coating
5. Soft bake
6. Exposure (193nm stepper)
7. Post exposure bake
8. Developement
9. BARC and Silicon etch (ICP)
10. Final Photonic wire

Mask technology

- CMOS reticles: 0.13um, 0.18um
- 5nm design grid
- 4X reduction litho
- Design rules
- Min feature size: 100nm (0.13um tech)
- Designers deliver GDSII data
- Fracturing (MEBES data)

10-30 designs

Geometric design data

4X

maskshop data

Fracturing
Increasing resolution

\[
\text{Resolution} = k_1 \frac{\lambda}{NA}
\]

Decrease illumination wavelength

- 365nm → 248nm → 193nm → 157nm → 13nm

Increase numerical aperture

- larger lenses → 0.85
- immersion: \( NA = n_{\text{medium}} \cdot \sin \theta_{\text{max}} \)

Technology Factor

- light source (coherency, off-axis illumination, ..)
- mask technology (phase shifting masks)
- mask correction (assist features, OPC)
imec technology: waveguides
Deep & Shallow etch

- reduce contrast locally
- keep light confined
- flatten phase fronts

-0.15dB loss per crossing
-40dB crosstalk

W. Bogaerts, OL 32, p.280
Arrayed Waveguide Grating

8-channel, 400GHz
FSR = 30nm
footprint = 200 x 350 µm²
- -25 dB crosstalk level
- -1 dB insertion loss (center channel)
- 1.5 dB non-uniformity
Reproducibility

18 identical AWGs
- shift in channel peak ~ 2.5nm
- strong correlation with location of the AWG on chip

Possible causes
- center-to-edge on wafer
- lithography scanning
- mask fabrication
- mask loading
Die to die uniformity

- Long range (few 10’s of mm) – device width and height
- Non-uniformity source – Litho, Etch, Wafer

<table>
<thead>
<tr>
<th>Distance between the devices (Die-to-Die)</th>
<th>Average resonance wavelength shift obtained (3 chips/12 devices)</th>
<th>Smallest resonance Wavelength shift obtained</th>
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<tbody>
<tr>
<td></td>
<td>Ring resonator</td>
<td>MZI</td>
</tr>
<tr>
<td>10,000mm</td>
<td>1.3nm</td>
<td>1.08nm</td>
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<tr>
<td>20,000mm</td>
<td>1.8nm</td>
<td>1.73nm</td>
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</table>

Transmission [dB] vs. Wavelength [nm]

- Die 1
- Die 2
- Die 3
- Die 4
- Die 5
- Die 6
- Die 7
- Die 8
- Die 9
- Die 10
- Die 11
- Die 12
Dose to target

• Each feature has a different dose-to-target

- iso line
- line pair (coupled WGs)
- dense line pair (slot waveguide)
- dense lines
- dense holes
Line width with exposure dose

Line width (nm) vs. Exposure dose (mJ) for different line widths:
- 200 nm
- 300 nm
- 400 nm
- 500 nm
- 600 nm
- 700 nm

Designed Line Width:
- Green line for 200 nm
- Blue line for 300 nm
- Green triangles for 400 nm
- Blue triangles for 500 nm
- Green squares for 600 nm
- Blue circles for 700 nm

Waveguide dimensions

Question:
- Given certain optimization criteria
- What is optimal **aspect ratio** for waveguide?

Popovic e.a.:
- Optimisation for:
  - Low loss,
  - Low sensitivity to dimensional variations
  - High thermal optic effect
- Choose AR = 6:1 !!!

Alternative optimisation criteria:
- High non-linear effects
- Optimized sensing (overlap with outside world)
  - Debackere, PhD thesis UGent (2010)
- Dispersion

Focusing grating couplers

Curved gratings: focus light in submicron waveguides

- No adiabatic transition needed
- Grating in linear taper
- Grating in slab, focus on low-contrast aperture

High-efficiency Fiber I/O

Grating coupler with locally thicker Si

More complex process required

Low loss

Limited bandwidth (40nm 1dB)

Novel packaging required

Wafer scale testing!

Poly-silicon overlay

Coupling efficiency = 68%

Thicker teeth

220nm Si

2µm SiO₂

silicon substrate

Insertion loss for 1 coupler [dB]

Wavelength [nm]
High efficiency fiber I/O

Inverted taper approach

- Mode is ‘squeezed out’ of core
- Captured by overlay waveguide
- Large bandwidth
- Low loss
- Low polarisation dependence
- Integration??
- High NA fiber

High NA fiber
inverted taper

to circuit
Carrier dispersion modulators

Create lateral p-n junction in the waveguide

- carrier injection changes refractive index
- lateral or vertical
- doping also causes absorption

Doping profile

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Contacting

- Need sufficiently thick top oxide (PMD)
- PMD thickness in 0.13-0.18um process: ~500nm
  → custom contact module with very different contact aspect ratio
- Inverted taper fiber I/O with thick cladding: integration challenge
Active devices

• Detectors & sources
  • Ge
    • Detectors
    • maybe sources (exploratory work)
  • III-V
    • Sources, detectors, modulators, switches, λ convertors, flip-flops, …

• III-V on Si integration on wafer scale?
  • Yes
  • Take care of contamination, contacting, integration
  • Today on chip scale and being scaled up
3D chip stacking

Technology in advanced stage

- Commercial 3D processes available
- imec: thin chip stacking
- ‘Cu nail’ TSV
Public offering

All of this in a process that:
• can be maintained
• can be monitored
• has sufficiently low cost for a given volume
• allows MPW implementation
• we can make a design kit for
WAFER TESTING
Wafer testing

Test structures for process monitoring/qualification

• What to measure?
• How to measure?
Wafer testing: testsuite

Structure metrology
• standard waveguide width
• standard coupler width/gap
• ...

Optical test structures
• waveguide losses
• fiber I/O efficiency
• standard filter characteristic (e.g. ring resonator)
• standard p(i)n junction performance
• .....
IMEC test suite

- Spirals
- MZIs
- MMIs
- Crossings
- Rings
How to measure

• Probe station
• Vertical fiber I/O
• Cost-effective or robust probes:
  • Standard single mode fibers (flexible use)
  • Fiber arrays (robust, multi I/O address)
Fabrication uniformity

Measurements: IR Camera setup

- Screen
- Infrared Camera
- Collimated IR beam from tunable laser

6mm
Measurements

All rows
DESIGN
Design flow

- EM/multiphysics/analytical simulation
- Layout
- DRC
- GDS
- User-foundry interface

Design rules document or limited PDK
Future design flow

Schematic

Place & route

Layout

LVS

DRC

Circuit simulation and verification

Design library
PDK
IP blocks

EM simulation

Extraction

Possible design service interface
Design automation

EM Simulation

Layout

Circuit simulation

Verification
Design automation

• Make photonic design tools talk to each other
• Make EDA tools address photonic engines/libraries
• Enable PDKs with device simulation models, …

Standard interface / API photonics design tools, engines, libraries

EDA tools

OpenAccess

Circuit simulation
EM, multiphysics simulation
Verification
Layout

PROTOTYPING
ePIXfab MPW

- Users send in design
- ePIXfab mask integration
- IMEC and LETI fabrication
- Wafers distributed

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<th>Sign-in</th>
<th>Mask</th>
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<th>Technology</th>
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Technology

• 200mm pilot lines
  • Continuous operation 24/24, 7/7
  • Trained operator force, dedicated support team, development team
  • Manufacturing execution system
• Well controlled environment
  • Strict contamination control
  • Statistical process control (electronics)
  • Procedures

• High-end tools
  • Deep submicron technology (0.18→90nm)
  • Wafer scale (200mm)
  • 193nm deep UV lithography
Public offering of fab process

Main questions:
• what is useful to the fabless researcher?
• how much are they willing to pay for it?
• cost control:
  • process running cost
  • process maintenance cost
  • manpower
• supply chain control
• risk control & mitigation

A process that makes fantastic devices is not necessarily a process that can be sustainably offered!
Silicon Photonics Forum
Building the food chain from research to the market

Friday 30 April 2010
imec auditorium, Leuven, Belgium
10h30 – 17h

• Learn about the fabless supply chain
• Discuss the future of fabless silicon photonics
• Silicon photonics tutorial 8h30-10h

Keynote: Cary Gunn, experiences from Genalyte and Luxtera
Speakers include PhoeniX, AMO, OptoCAP, DAS photonics, KTH, XiO,TU Berlin, NTU Athens, PoliMi, imec, …

Registration & venue: www.epixfab.eu