A 5-MHz 11-bit Delay-Based Self-Oscillating $\Sigma\Delta$ Modulator in 0.025 mm^2

Bart De Vuyst, Pieter Rombouts

This document is an author's draft version submitted for publication the IEEE CICC conference 2010,
The actual version was published as:

Bart De Vuyst, Pieter Rombouts, "A 5-MHz 11-bit Delay-Based Self-Oscillating $\Sigma\Delta$ Modulator in 0.025 mm^2," IEEE Custom Integrated Circuits Conference (CICC), 19-22 Sept. 2010, San Jose, USA

A 5-MHz 11-bit Delay-Based Self-Oscillating $\Sigma\Delta$ Modulator in 0.025 mm^2

Bart De Vuyst, Pieter Rombouts
Ghent University (UGent), Dept. ELIS, Sint-Pietersnieuwstraat 41, 9000 Ghent, Belgium
Email: bart.devuyst,rombouts@elis.UGent.be

***Abstract*—In this paper a self-oscillating $\Sigma\Delta$ modulator is presented. By introducing this self-oscillation in the system, the loop filter operates at a speed significantly lower than dictated by the clock frequency. This allows for a simple and power efficient design of the opamps used in the loop filter. The self-oscillation is induced here by introducing a controlled delay in the feedback loop of the modulator. A second order CMOS prototype was constructed in a 0.18 µm technology. A clock frequency of 850 MHz generates a self-oscillation mode at 106.25 MHz. The modulator achieves a dynamic range (DR) of 66 dB for a signal bandwidth of 5 MHz. The power consumption is only 6 mW and the chip area of the modulator core is 0.025 mm^2.**

I. Introduction

$\Sigma\Delta$ modulators are known to realize high resolution analog-to-digital (A/D) converters. To increase the bandwidth and reduce the power consumption of these converters, continuous-time (CT) $\Sigma\Delta$ modulators have proven to be a good solution. In contrast to discrete-time (DT) $\Sigma\Delta$ modulators, here the unity gain-bandwidths (GBWs) of the opamps used in the loop filter only have to exceed the sample frequency f_s by a factor 2 or less. This way higher sample frequencies can be used and the bandwidth can be extended into the wide MHz range.

To achieve these high bandwidths, usually a low oversampling ratio (OSR) is combined with a multibit quantizer [1], [2]. However, as the number of comparators rises exponentially with the number of bits in a flash quantizer, this increases both chip area and circuit complexity [3]. Furthermore, also a multibit digital-to-analog converter (DAC) has to be included. As this DAC is situated in the feedback path its linearity must at least be equal to the modulator's resolution. Therefore typically dynamic element matching (DEM) techniques are required. CT $\Sigma\Delta$ modulators are also sensitive to clock jitter when using non-return-to-zero (NRZ) or return-to-zero (RZ) pulses in the feedback DAC. This gives rise to extra jitter noise in the signal band [4].

Recently, time-encoding has shown to be a promising technique to avoid multibit quantization [5], [6]. The input is thereby encoded into the output signal through pulsewidth modulation. For this purpose we consider a CT $\Sigma\Delta$ modulator which operates in a self-oscillating mode in this paper. The self-oscillating frequency is an integer fraction of the sample frequency f_s. It is controlled by introducing a digital delay in the feedback path. This way the system globally works at a much lower speed than f_s and the opamp GBWs are significantly relaxed. Jitter sensitivity is also heavily reduced as the feedback DAC signal toggles at a lower rate. Also, only a 1-bit quantizer (comparator) and feedback DAC are required.

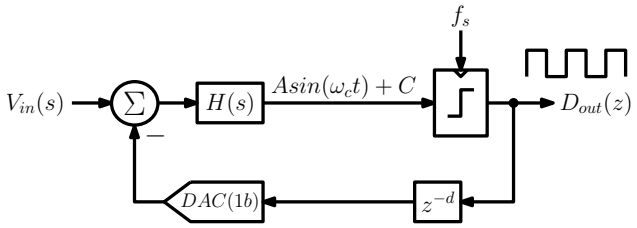

Fig. 1. Block diagram of a delay-based self-oscillating $\Sigma\Delta$ modulator.

II. Delay-Based Self-Oscillating CT $\Sigma\Delta$ Modulator

Fig. 1 shows the basic architecture for the delay-based self-oscillating $\Sigma\Delta$ modulator. It consists of a loop filter $H(s)$, a comparator clocked at f_s, a single-bit feedback DAC and a digital delay of d clock cycles. In [7] a similar system is presented, except for the fact that a hysteresis based comparator is used to induce self-oscillation in the $\Sigma\Delta$ loop. However, the rest of the analysis made there remains valid for the delay-based modulator.

The system shown in fig. 1 is non-linear due to the presence of the comparator and therefore hard to analyze. In [8] the describing-function theory is proposed as a way to linearize these systems. The system is described by considering the behaviour for a superposition of different kinds of signals at the comparator input. For each type of these signals the comparator is linearized. In this case the comparator input can contain two types of signals: a first contribution from the self-oscillating output and a second contribution originating from the input signal $V_{in}(s)$.

A. System Behaviour for the Self-Oscillation Mode

We assume a zero input when investigating the system behaviour for the self-oscillation mode. The output signal is then a square wave signal of frequency f_c. This signal is low-pass filtered through the loop filter $H(s)$. Therefore only the first order harmonic is accounted for in fig. 1. A sine wave with amplitude A and frequency $\omega_c = 2\pi f_c$ appears at the input of the quantizer. In [8] it is now stated that the quantizer can be replaced by a linear gain which depends on the amplitude A

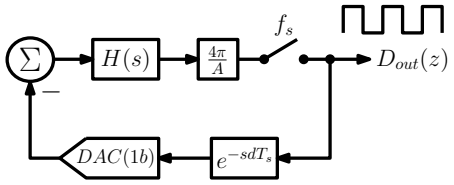

Fig. 2. Behaviour of the system for the self-oscillation.

of this sine wave (see fig. 2). The equivalent comparator gain equals:

$$G_{C,SO} = \frac{4}{\pi A} \tag{1}$$

As we now have a fully linear loop, the digital delay can be replaced by analog phase shift e^{-sdT_s}. A neccessary condition for the sine wave to reappear at the input of the comparator is now that the combination of the loop filter, the delay, the DAC pulse and the sampler give rise to a 180 °phase shift for the frequency f_c. Due to the presence of the sampler the oscillation frequency can only be an integer fraction of the sample frequency [7]. This condition results in a solution for A, the amplitude of the self-oscillating signal, which can be used to determine the equivalent comparator gain.

B. System Response to the Input Signal

A linearization of the comparator can also be performed when considering the contribution of the input signal to the comparator input. The assumption made here is that the input signal is very low-frequent compared to the self-oscillation, so that the contribution of the input signal in fig. 1 can be considered to be a DC value C. The equivalent comparator gain now equals:

$$G_{C,in} = \frac{2}{\pi A} \tag{2}$$

This is only half the value as it was for the self-oscillation mode and is still dependent on the amplitude A of the self-oscillating signal. In fig. 3 the situation is depicted. The input now modulates the self-oscillation in pulsewidth. As the sampler is still present, the pulsewidth can only be modulated in discrete steps of the sampling period T_s. This can be seen as a quantization error similar to a conventional multibit quantizer. The presence of the low-pass loop filter makes sure this quantization error is suppressed in the signal band.

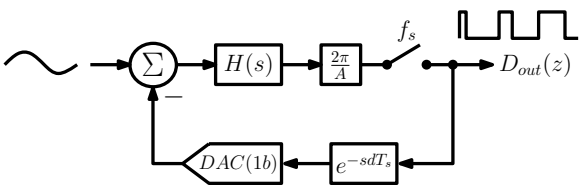

Fig. 3. Behaviour of the system for the low-frequency input signal.

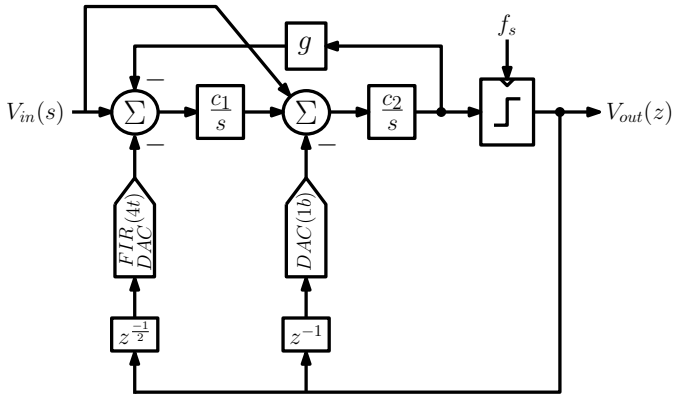

Fig. 4. Block diagram of the self-oscillating ΣΔ modulator.

C. Comparison to a Conventional ΣΔ Modulator

An interesting point of view is the comparison of this system to a conventional ΣΔ modulator. As already stated when applying zero input the system generates a self-oscillating signal of frequency f_c. This can be seen as a limit cycle generated by a conventional ΣΔ modulator operating at a clock frequency of $2f_c$. An equivalent OSR can be determined for the signal bandwidth f_b:

$$\text{OSR} = \frac{f_c}{f_b} \tag{3}$$

The pulsewidth modulation of the self-oscillating output by the input signal can be seen as an equivalent multibit quantizer with a number of levels equal to $\frac{f_s}{f_c}$.

III. System Level Design

In fig. 4 the block diagram of the implemented system is shown. It consists of a second order loop filter with local feedback for zero spreading. The self-oscillation frequency, which is at a relative high frequency compared to the integrator coefficients, is mainly determined by the first-order inner loop. One unit delay is introduced to supply enough phase shift for oscillation at $\frac{f_s}{8}$. This way, when applying zero input, the output signal only toggles once every 4 clock cycles. The outer loop has a half clock cycle delay to relax the settling of the comparator. Also, a uniform 4-tap finite-impulse-response (FIR) DAC is included here:

$$H_{FIRDAC}(z) = \frac{1}{4}\left(1 + z^{-1} + z^{-2} + z^{-3}\right) \tag{4}$$

Jitter sensitivity is further reduced this way. Finally, a feed-in path from the input is also present to reduce to output swing of the first integrator.

As such the system behaves similar to a conventional ΣΔ modulator with clock frequency $\frac{f_s}{4}$ and a 3-bit quantizer. The signal bandwidth f_b is fixed at $\frac{f_s}{170}$. The equivalent OSR becomes 21.25. The resulting system parameters are shown in table I.

A simulated output spectrum is shown in fig. 5. A -4.3 dB input relative to full scale (dBFS) is applied. The input frequency equals $\frac{f_b}{5}$. The edge of the signal band and the

TABLE I
SELF-OSCILLATING ΣΔ MODULATOR SYSTEM PARAMETERS

Parameter	System level value	Circuit level value
c_1	$0.05 f_s$	42.5 MHz
c_2	$0.05 f_s$	42.5 MHz
g	0.0046	0.0046
f_s		850 MHz
f_c	$f_s/8$	106.25 MHz
f_b	$f_s/170$	5 MHz
OSR	21.25	21.25

nominal oscillation frequency are indicated by the two vertical lines. Clearly the output contains a lot of content around the oscillation frequency. Due to the pulsewidth modulation of the oscillation mode by the input, spectral broadening appears around $\frac{f_s}{8}$. The resulting signal-to-noise ratio (SNR) equals 64.5 dB. Because of the nonlinear nature of the system, a third order harmonic is also present at -78 dB relative to the carrier (dBc).

IV. CIRCUIT LEVEL DESIGN

A CMOS prototype is designed in a 0.18 µm technology. A clock frequency of 850 MHz is chosen, based on the minimum required settling time for the comparator. This way the oscillation frequency f_c equals 106.25 MHz and the signal bandwidth f_b equals 5 MHz. All the actual values of the significant system parameters on the circuit level can also be found in table I.

The system is implemented using fully differential circuits. The integrators are formed with active-RC feedback opamps. Due to the resistive loads a two-stage Miller compensated opamp topology is used for both integrators. Fig. 6 shows the schematic of this opamp. A series resistor R_z is included with the compensation capacitor C_C to cancel the effect of a right-halfplane zero. The common-mode feedback (CMFB) control signal is applied at the NMOS transistors in the first stage. The common-mode voltage is sensed with a resistive voltage

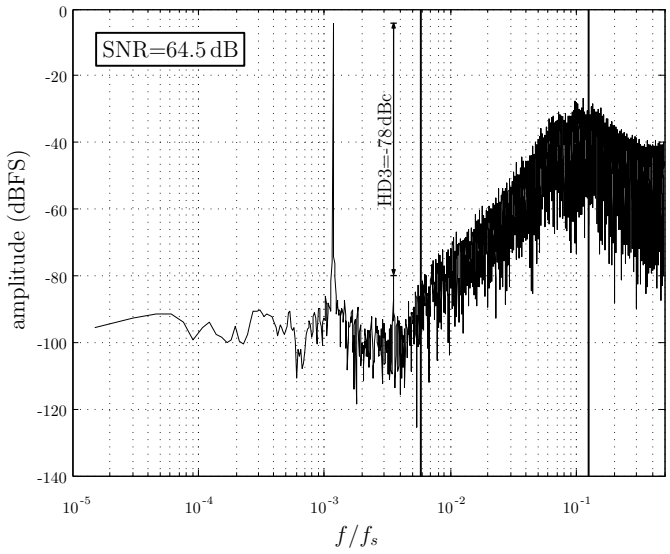

Fig. 5. Simulated output spectrum for a -4.3 dBFS input signal at $f_b/5$.

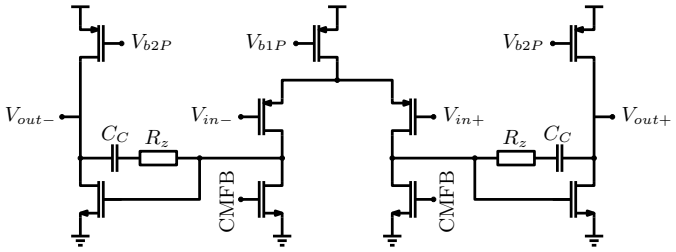

Fig. 6. Miller compensated two-stage operational amplifier used for the integrators.

divider at the outputs (not shown in fig. 6) and compared to a reference value using an auxiliary amplifier.

The feedback signals are implemented using resistive DACs. They are digitally controlled by standard cell flipflops. The comparator is implemented as a pre-amplifier followed by a latch. The pre-amplifier is a simple PMOS differential pair loaded with ordinary active load NMOS transistors, very similar to what was used in [9].

V. EXPERIMENTAL RESULTS

Fig. 7 shows a microphotograph of the prototype chip fabricated in a single-poly six-metal layer 0.18 µm digital CMOS process. The modulator core area is only 0.025 mm^2. The power consumption is 6 mW from a 1.8 V supply voltage for f_s equal to 850 MHz. 85 % of the power is consumed in the analog parts of the chip and only 15 % in the digital control for the feedback DACs.

A measured output spectrum is shown in fig. 8. The input conditions are equal to the ones from fig. 5 (-4.3 dBFS input tone at 1 MHz). A full scale input corresponds to a sine wave with an amplitude of 1.8 V. High correlation between the measured spectrum and the simulated spectrum can be observed. The resulting SNR equals 61.1 dB now. Also second-order and third-order distortion appear at -57 dBc and -70 dBc respectively. Especially the second-order distortion is worrying as it limits the signal-to-noise and distortion ratio (SNDR) of the modulator. Imbalance in the differential behaviour of the system, more precisely rise and fall time issues in the standard cell flipflops seemed to be the cause of this distortion. However, this is a non fundamental problem which could be fixed in future designs.

In fig. 9 the SNR, SNDR and the SNDR without the inclusion of the second-order distortion is shown in function

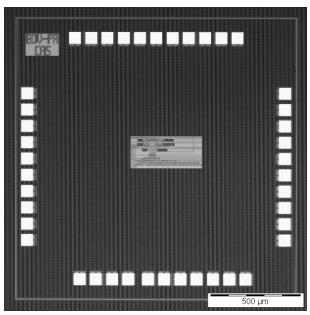

Fig. 7. Microphotograph of the 0.18 µm CMOS prototype.

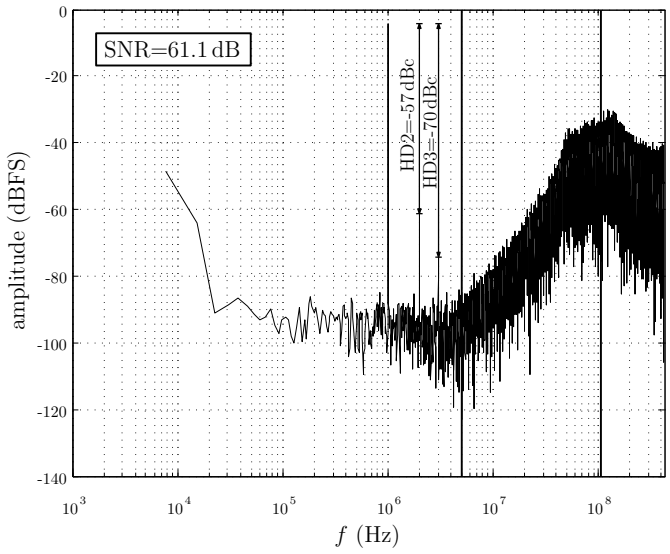

Fig. 8. Measured output spectrum for a 1 MHz, -4.3 dBFS input signal.

of the input amplitude. The peak SNR of 61.1 dB is found for the -4.3 dBFS input. Even for a full scale input the SNR is still 50,2 dB. However, distortion becomes quite large then, which lowers the SNDR to 41.8 dB. As one can see second-order distortion is clearly dominant as the SNDR already starts dropping at much lower input signal levels compared to the situation where second-order distortion was neglected. The dynamic range of the modulator equals 66 dB which corresponds to an 11-bit resolution. Based on the power consumption we can estimate a figure of merit (FOM) for our prototype:

$$\text{FOM} = \frac{P}{2 f_b 2^B} \tag{5}$$

This FOM equals 360 fJ/conversion step for our design.

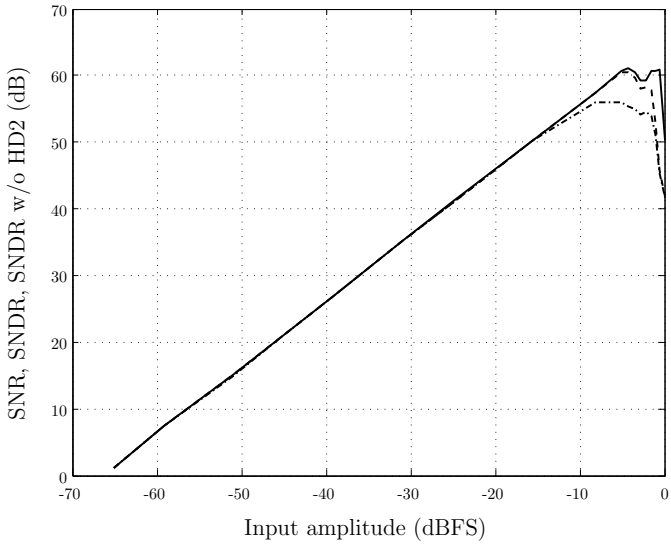

Fig. 9. SNR (solid), SNDR (dashed-dotted) and the SNDR without second order distortion (dashed) in function of the input amplitude.

VI. Conclusion

In this paper a second order self-oscillating $\Sigma\Delta$ modulator fabricated in a 0.18 µm CMOS process was presented. The introduction of a controlled delay in the feedback loop causes the system to oscillate at 106.25 MHz for a clock frequency of 850 MHz. The modulator achieves a dynamic range (DR) of 66 dB for a signal bandwidth of 5 MHz. This corresponds to an 11-bit resolution. Due to the simplicity of the circuit, the modulator core area is only 0.025 mm^2. The power consumption of the modulator is 6 mW resulting in a FOM of 360 fJ/conversion step.

VII. Acknowledgement

This work was supported by the Fund for Scientific Research (F.W.O.-Vlaanderen, Belgium).

References

[1] G. Mitteregger, C. Ebner, S. Mechnig, T. Blon, C. Holuigue, and E. Romani, "A 20-mW 640-MHz CMOS Continuous-Time $\Sigma\Delta$ ADC With 20-MHz Signal Bandwith, 80-dB Dynamic Range and 12-bit ENOB," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2641–2649, 2006.

[2] Patón, S. and Di Giandomenico, A. and Hernández, L. and Wiesbauer, A. and Pötscher, T., "A 70-mW 300-MHz CMOS Continuous-Time $\Sigma\Delta$ ADC With 15-MHz Bandwidth and 11 Bits of Resolution," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1056–1062, 2004.

[3] J. De Maeyer, P. Rombouts, and L. Weyten, "Efficient Multibit Quantization in Continuous-Time $\Sigma\Delta$ Modulators," *IEEE Trans. Circuits Syst.-I*, vol. 54, no. 4, pp. 757–767, Apr. 2007.

[4] K. Reddy and S. Pavan, "Fundamental limitations of continuous-time delta-sigma modulators due to clock jitter," *IEEE Trans. Circuits Syst.-I*, vol. 54, no. 10, pp. 2184–2193, 2007.

[5] E. Prefasi, L. Hernandez, S. Paton, A. Wiesbauer, R. Gaggl, and E. Pun, "A 0.1 mm^2, Wide Bandwith Continuous-Time $\Sigma\Delta$ ADC Based on a Time Encoding Quantizer in 0.13-µm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2745–2754, 2009.

[6] F. Colodro and A. Torralba, "New continuous-time multibit sigma-delta modulators with low sensitivity to clock jitter," *IEEE Trans. Circuits Syst.-I*, vol. 56, no. 1, pp. 74–83, 2009.

[7] S. Ouzounov, A. Hegt, and A. van Roermund, "Sigma-delta modulators operating at a limit cycle," *IEEE Trans. Circuits Syst.-II*, vol. 53, no. 5, pp. 399–403, 2006.

[8] A. Gelb and W. E. Vander Velde, *Multiple-Input Describing Functions and Nonlinear System Design*. McGraw-Hill, 1968.

[9] P. Rombouts, W. De Wilde, and L. Weyten, "A 13.5-b 1.2-v micropower extended counting a/d converter," *IEEE J. Solid-State Circuits*, vol. 36, no. 2, pp. 176–183, 2001.